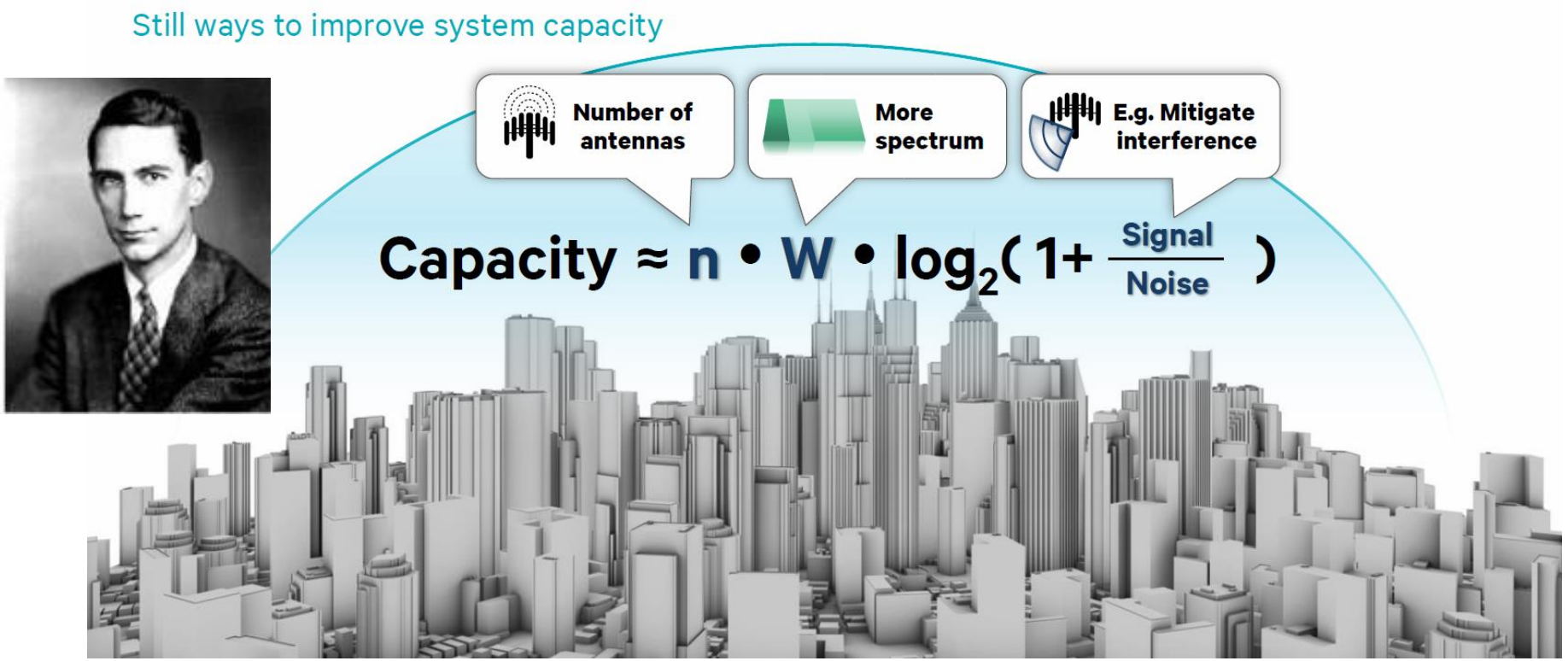
5G載波聚合基本觀念

元智大學 李建育助理教授

Agenda

- Carrier aggregation
- RF aspects of carrier aggregation
- New topic of carrier aggregation

Shannon's Law



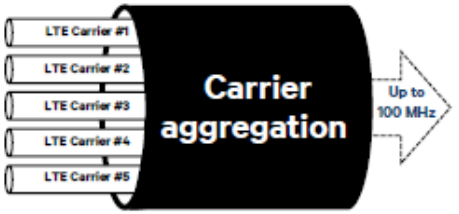
- *Increase number of antennas* : MIMO, Massive MIMO,…
- *Increase bandwidth* : Carrier aggregation, towards millimeter-wave,…
- *Improve SNR* : eICIC, antenna array,…

[Ref] : "LTE Advanced – Evolving and expanding in to new frontiers", Qualcomm, Aug. 2014

LTE Advanced brings different dimensions of improvements

Leverage wider bandwidth

Carrier aggregation across multiple carriers, multiple bands, and across licensed and unlicensed spectrum



Higher data rates
(bps)

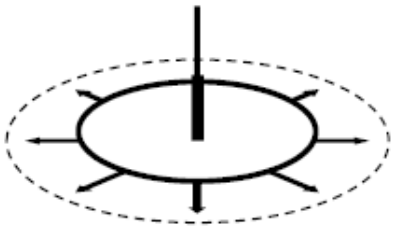
Leverage more antennas

Downlink MIMO up to 8x8, enhanced Multi User MIMO and uplink MIMO up to 4x4

Higher spectral efficiency
(bps/Hz)

Leverage HetNets

With advanced interference management (FeICIC/IC)



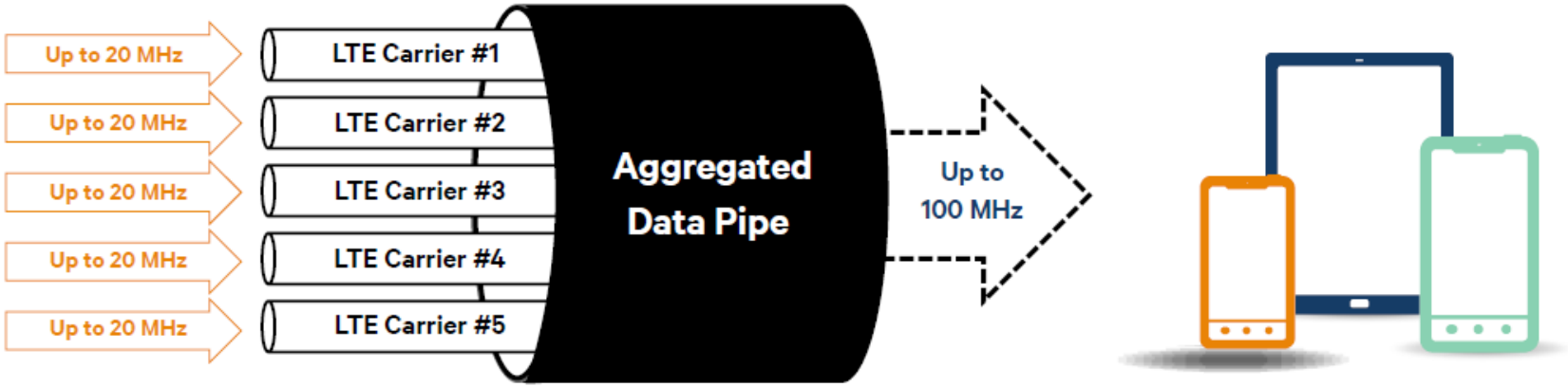
Small Cell Range Expansion

Higher spectral efficiency per coverage area
(bps/Hz/km²)

[Ref] : "LTE Advanced – Evolving and expanding in to new frontiers", Qualcomm, Aug. 2014

Carrier aggregation is the first step of LTE-A

- Motivation
  - Higher peak data rates.
  - Facilitate efficient use of fragmented spectrum.
- Bandwidth extension by aggregating LTE component carriers (CC).
  - Up to 5 CC can be allocated in both DL and UL – 100 MHz aggregated.
  - Components carriers are backwards compatible with Release 8 terminals.
  - Symmetric or asymmetric DL/UL CA configurations.

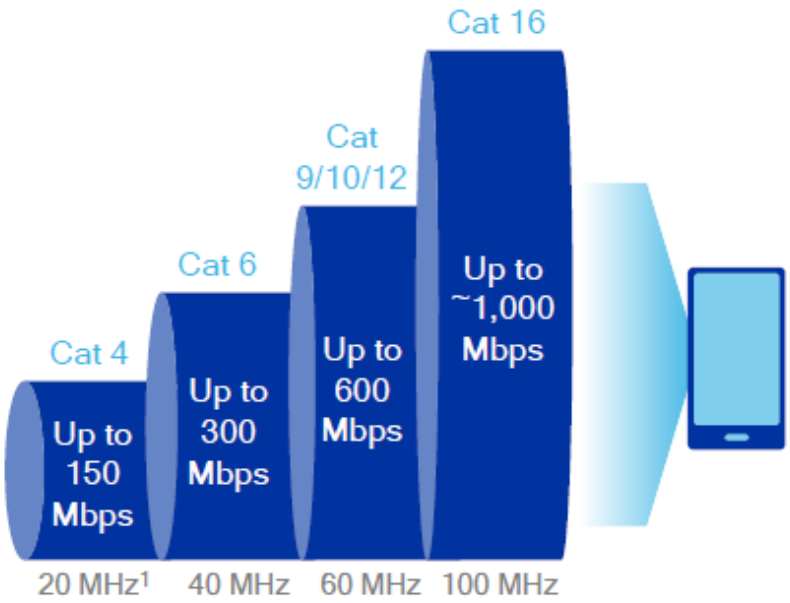


[Ref] : "LTE Advanced – Evolving and expanding in to new frontiers", Qualcomm, Aug. 2014
[Ref] : "Carrier Aggregation : Fundamentals and Deployments", Keysight Technologies, 2014

Evolving Carrier Aggregation for faster data rates

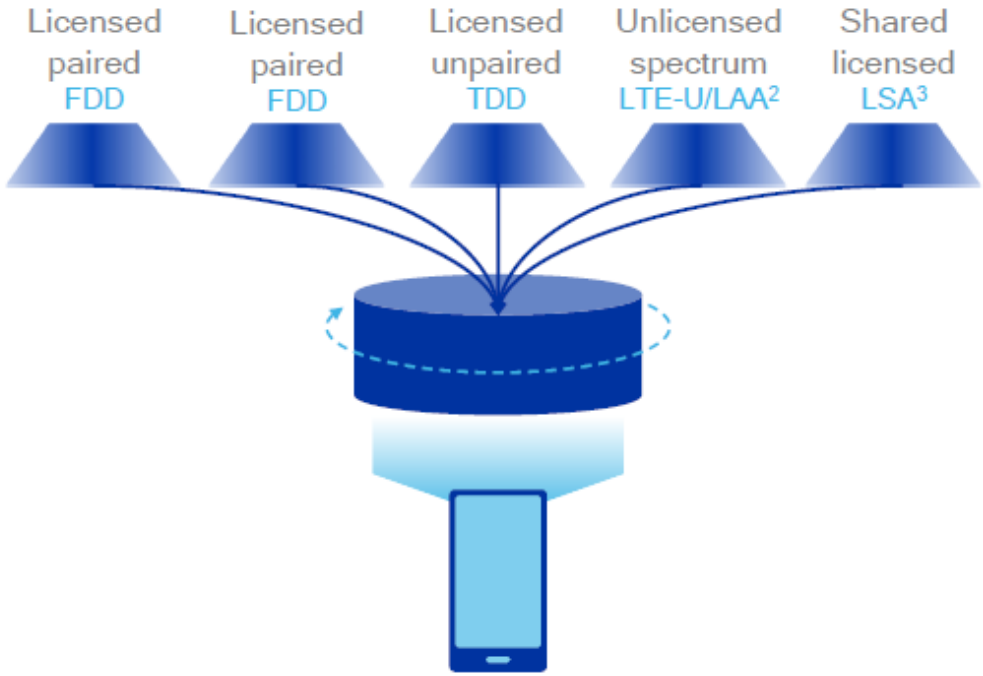
Enable mobile operators to maximize use of spectrum assets

Across more carriers



Note: UE category bandwidth shown are for 2x2 MIMO implementation; 256-QAM for Cat 11 and above

Across diverse spectrum types



[1] 10 + 10 CA; [2] LTE-U extends LTE to unlicensed spectrum, based on 3GPP Rel. 12 and supports migration to 3GPP Rel. 13 Licensed Assisted Access (LAA); [3] Licensed Shared Access

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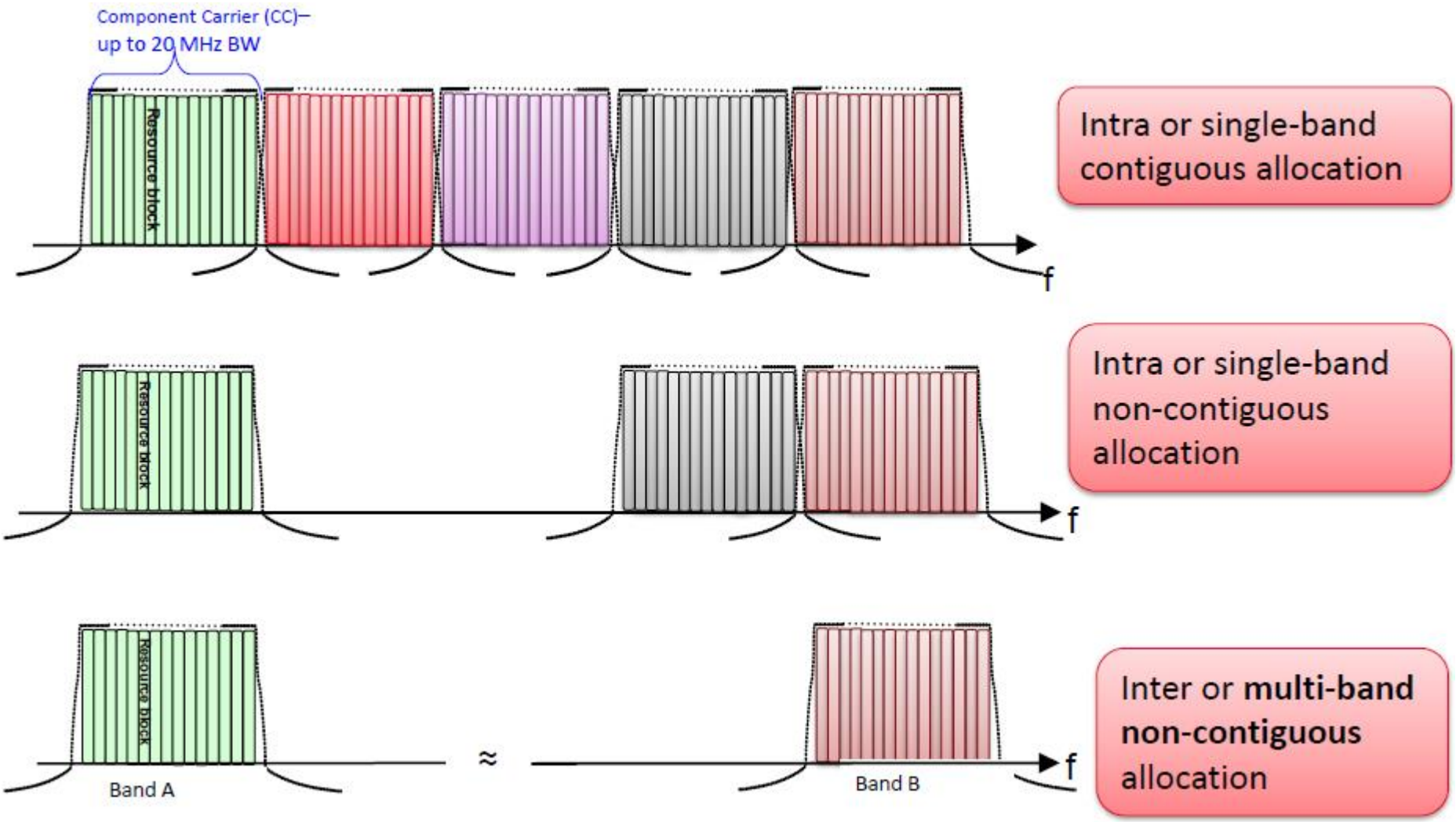
LTE-A feature – Carrier Aggregation (CA)



[Ref] : "Carrier Aggregation : Fundamentals and Deployments", Keysight Technologies, 2014

Relating FDD and TDD to CA

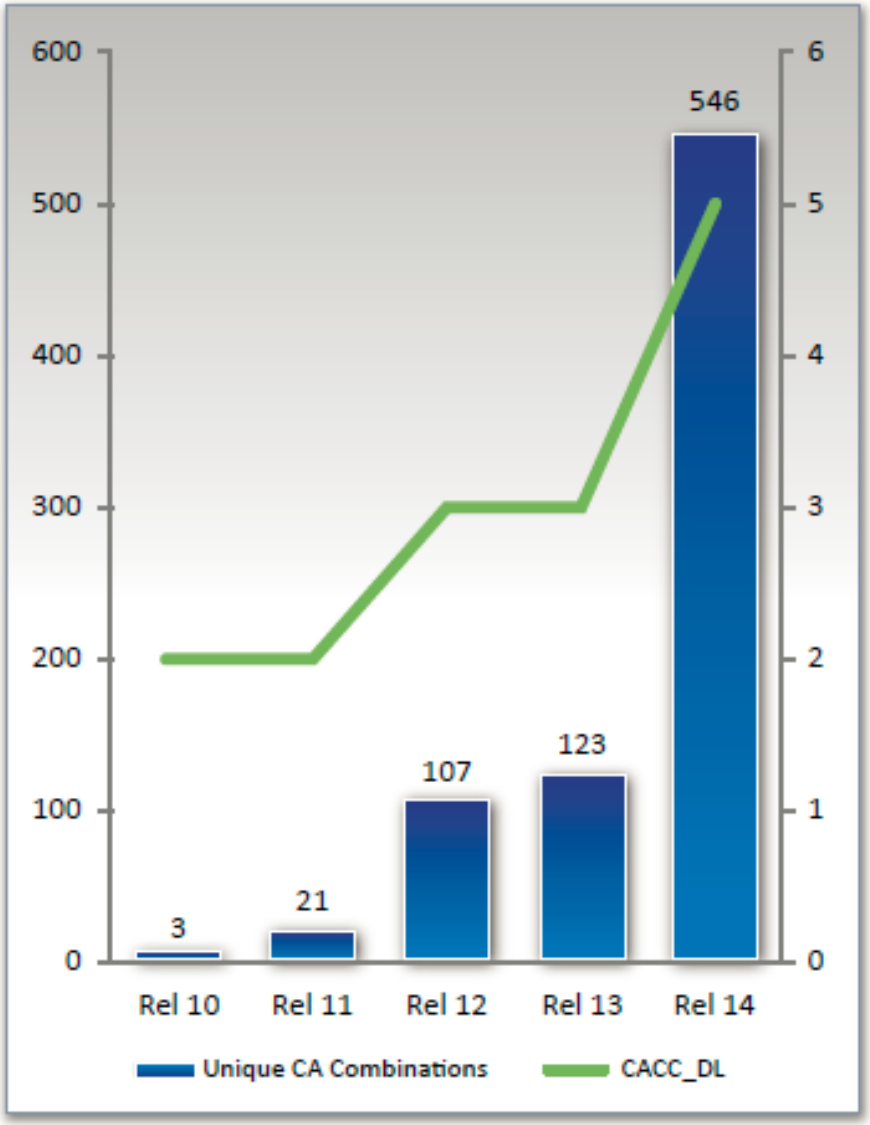
- In TDD :
  - The *bandwidth* and *number* of CCs must be the same for both the uplink and downlink.
- In FDD :
  - Downlink and uplink can be configured with a *different number* of CCs and *different bandwidths* in each (known as asymmetric configuration).
  - The number of uplink CCs cannot exceed the number of downlink CCs.
  - CA in FDD improves coverage and data rates.
- 3GPP defined FDD-TDD aggregation in Release 12, which allows either FDD or TDD as the primary cell. FDD-TDD aggregation can provide an attractive combination of low-band FDD for good coverage and high-band TDD with more spectrum for higher data rates.

LTE Carrier Aggregation Band Map

qorvo

2015	2016
B3+7 B3+20 B7+20	3CA B3+3+7 B7+7+3
B39+41 B1+3 B39 B40 B41 B3	CM UL B3+26 B3+41
B1+3 B1+5 B3+8 B1+7	3CA B1+3+5 B1+3+8 B1+5+7
B1+19 B3+19 B1+41 B1+8	B41+42 3CA B1+19+21 B1+42+42
B3+28 B3+5 B40	B7+28 3CA B3+7+28 B3+40+40
B4+13 B4+12 B2+4 B41+41	3CA 4+13+LTE-U (DL) B12+30+2 B41+41+41 B66

CA Component Carriers and Combinations (Sub 6 GHz)



Carrier Aggregation in Taiwan

CA類型	CA組合	適用業者
2 CA	B3+B7	中華電信、遠傳電信
	B3+B8	中華電信
	B3+B28	遠傳電信、台灣大哥大
	B7+B8	中華電信、台灣之星
	B7+B28	遠傳電信、台灣大哥大
	B28+B38(B41)	亞太電信
	B1+B3	中華、遠傳、台灣大哥大
	B1+B7	中華電信、遠傳電信
	B1+B8	中華電信
3CA	B3+B7+B8	中華電信
	B3+B3+B8	中華電信
	B3+B3+B7	中華電信
	B3+B7+B7	中華電信
	B3+B7+B8	中華電信
	B7+B7+B8	中華電信
	B3+B7+B28	遠傳電信
	B1+B3+B3	中華電信
	B1+B3+B8	中華電信
	B1+B7+B7	中華電信
	B1+B3+B7	中華電信、遠傳電信
	B1+B3+B28	遠傳電信、台灣大哥大
	B8+B28+B38(B41)	亞太電信
4CA	B3+B3+B7+B7	中華電信
	B1+B3+B3+B7	中華電信
	B1+B3+B7+B7	中華電信
	B1+B3+B7+B8	中華電信
	B1+B3+B3+B8	中華電信
	B3+B3+B7+B7	中華電信
	B1+B3+B7+B28	遠傳電信
5CA	B3+B3+B7+B7+B8	中華電信
	B1+B3+B3+B7+B7	中華電信

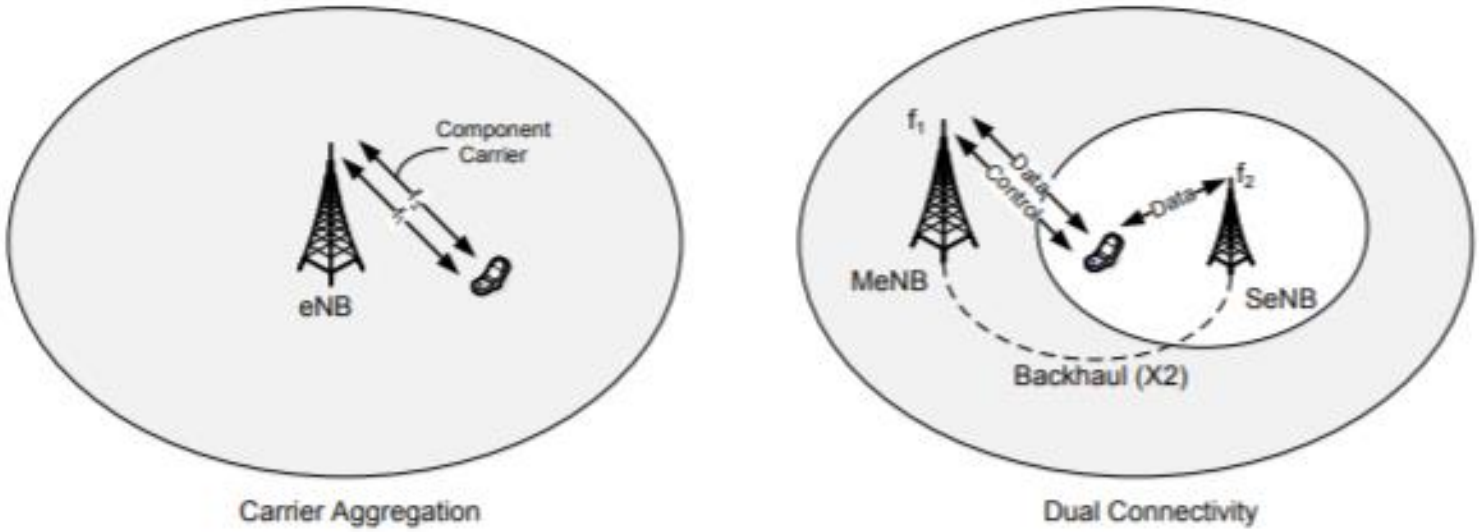
5G NR & 4G LTE

	5G New Radio (Release 15)	LTE-Advanced Pro (Release 13 & 14)	LTE-Advanced (Release 10 to 12)
User Data Rate	> 10 Gbps	> 3 Gbps	> 1 Gbps
Latency	> 1ms	> 2ms	~10 ms
Frequency Support	Up to 40 GHz	Up to 6 GHz	Up to 6 GHz
Channel Bandwidth	Up to 500 MHz	Up to 20 MHz	Up to 20 MHz
Max carriers	16 (LTE + NR)	32	5
Max Bandwidth	1000 MHz	640 MHz	100 MHz
MIMO antennas	64 to 256	32	8
Spectrum Sharing	mmWave & NR Dual Connectivity NR-based LAA+ NR MulteFire LTE-U	LAA / eLAA LWA MulteFire CBRS / LSA LTE-U	LTE-U (Rel. 12)

[Ref] : https://www.androidauthority.com/5g-vs-gigabit-lte-843341/

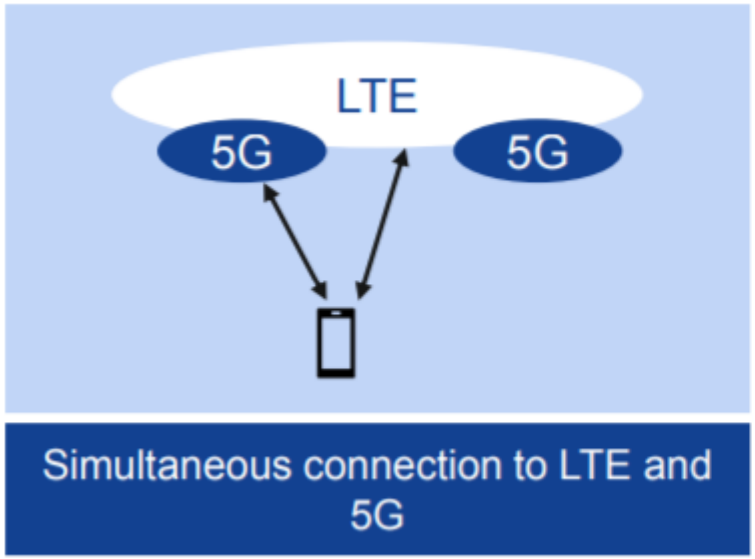
Dual Connectivity (DC)

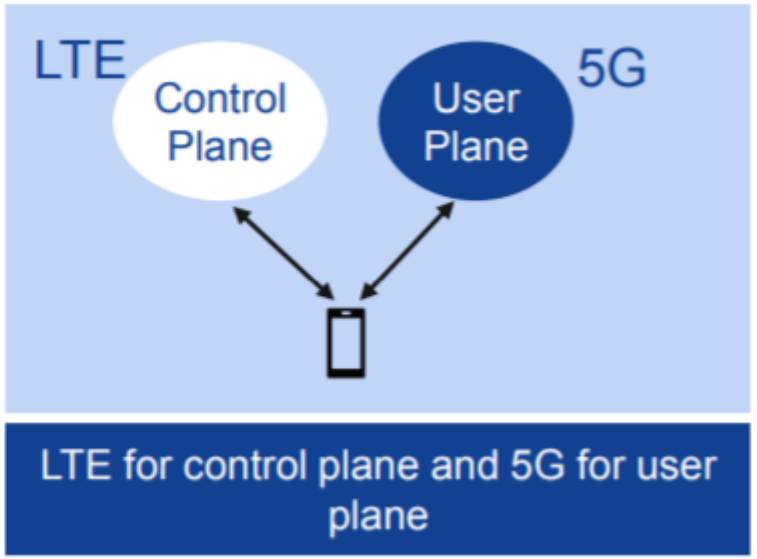
- DC : introduced in 3GPP to allow a UE to simultaneously transmit and receive data on multiple component carriers from two cell groups via master eNB (MeNB) and secondary eNB (SeNB).
  - DC can increase user throughput, provide mobility robustness, and support load-balancing among eNBs



LTE – NR Dual Connectivity

- Stand-alone NR :
  - UE accesses standalone NR carrier and may not be connected to an LTE carrier.
- Non stand-alone NR (dual connectivity of LTE and NR) :
  - UE accesses LTE PCell, then is configured by dual connectivity to also operate on NR.





Global Bands, CA and Features

Region	Deployed	Planned
Europe	3CC_CA, UL 2CC_CA B1, B3, B7, B20, B28, B38	4CC_CA, LAA, L+L CA B40, B46, n28, n78
China	3CC_CA, UL 2CC_CA B1, B3, B5, B8, B39, B40, B41	UL 3CC_CA, 4x4 MIMO, HPUE B38, n78, n79
South Korea	5CC_CA, UL 2CC_CA, 4x4 MIMO B1, B3, B5, B7, B8	LAA B46, n78, n257
Japan	4CC_CA, 4x4 MIMO B1, B3, B11, B18, B19, B21, B26, B28, B41, B42	5CC_CA, UL 2CC_CA, HPUE n77, n79, n257
Australia	B1, B3, B5, B8, B40, B41	2CC_CA
U.S.	4CC_CA, 4x4 MIMO, LAA, HPUE B4/66, B5, B12, B13, B2, B30, B41, B46, B71	>5CC_CA, UL 2CC_CA, CBRS B14, B48, n71, n41, n257, n260

[Ref] : https://www.qorvo.com/applications/mobile-products/carrier-aggregation

5G NR spectrum (cont.)

FR1 (<6GHz)

NR operating band	Uplink (UL) operating band BS receive / UE transmit F_{UL_low} – F_{UL_high}	Downlink (DL) operating band BS transmit / UE receive F_{DL_low} – F_{DL_high}	Duplex Mode
n1	1920 MHz – 1980 MHz	2110 MHz – 2170 MHz	FDD
n2	1850 MHz – 1910 MHz	1930 MHz – 1990 MHz	FDD
n3	1710 MHz – 1785 MHz	1805 MHz – 1880 MHz	FDD
n5	824 MHz – 849 MHz	869 MHz – 894 MHz	FDD
n7	2500 MHz – 2570 MHz	2620 MHz – 2690 MHz	FDD
n8	880 MHz – 915 MHz	925 MHz – 960 MHz	FDD
n20	832 MHz – 862 MHz	791 MHz – 821 MHz	FDD
n28	703 MHz – 748 MHz	758 MHz – 803 MHz	FDD
n38	2570 MHz – 2620 MHz	2570 MHz – 2620 MHz	TDD
n41	2496 MHz – 2690 MHz	2496 MHz – 2690 MHz	TDD
n50	1432 MHz – 1517 MHz	1432 MHz – 1517 MHz	TDD
n51	1427 MHz – 1432 MHz	1427 MHz – 1432 MHz	TDD
n66	1710 MHz – 1780 MHz	2110 MHz – 2200 MHz	FDD
n70	1695 MHz – 1710 MHz	1995 MHz – 2020 MHz	FDD
n71	663 MHz – 698 MHz	617 MHz – 652 MHz	FDD
n74	1427 MHz – 1470 MHz	1475 MHz – 1518 MHz	FDD
n75	N/A	1432 MHz – 1517 MHz	SDL
n76	N/A	1427 MHz – 1432 MHz	SDL
n77	3300 MHz – 4200 MHz	3300 MHz – 4200 MHz	TDD
n78	3300 MHz – 3800 MHz	3300 MHz – 3800 MHz	TDD
n79	4400 MHz – 5000 MHz	4400 MHz – 5000 MHz	TDD
n80	1710 MHz – 1785 MHz	N/A	SUL
n81	880 MHz – 915 MHz	N/A	SUL
n82	832 MHz – 862 MHz	N/A	SUL
n83	703 MHz – 748 MHz	N/A	SUL
n84	1920 MHz – 1980 MHz	N/A	SUL

FR2 (24.25GHz – 52.6GHz)

n257	26500 MHz – 29500 MHz		26500 MHz – 29500 MHz		TDD
n258	24250 MHz – 27500 MHz		24250 MHz – 27500 MHz		TDD
n260	37000 MHz – 40000 MHz		37000 MHz – 40000 MHz		TDD

FR1: 26 new NR bands (450MHz-6000MHz)

- <1GHz: 600MHz, 700MHz
- <3GHz: LTE band re-farming
- 3 – 6GHz: highest global interest bands:
  n77 & n78 (3.3-4.2GHz)
  (100MHz BW)

FR2: 3 new NR bands (24.5 – 52.6GHz)

- Suitable for hotspot coverage , high capacity
- Highest interest
  n257 & n258 (24.25-29.5GHz)
  (400MHz BW)

3GPP TS 38.101-3 version 15.2.0 Release 15

- Status of carrier aggregation
- RF aspects of carrier aggregation
- New topic of carrier of carrier aggregation

Design Challenges

- Inter-band Carrier Aggregation

Class	Description
A1	Low-high band combination without harmonic relation between bands or intermodulation problem
A2	Low-high band combination with harmonic relation between bands
A3	Low-low or high-high band combination without intermodulation problem (low order IM)
A4	Low-low or high-high band combination with intermodulation problem (low order IM)
A5	Combination for A1-A4

- **A2** : Harmonics may cause degradation in the performance of the high band receiver.
- **A3** : The use of diplexers to split and combine RF chains are very challenging

Understanding downlink challenges

- Downlink sensitivity.
- Harmonic generation.
- Desense challenges in CA RF radio design.

Addressing Intra-Band uplink challenges

- In the China market, TDD is the main driver for UL carrier aggregation.
- In 2014, China Telecom and Nokia Networks announced the world's first FDD-TDD CA device chipsets. This development uses FDD Band 3 for improving LTE coverage and TDD Band 41 for improving throughput.
- Two issues are concerned here :
  - *Maximum Power Reduction*
  - *Linearity.*

Recognizing Inter-Band uplink challenges

- Inter-band uplink CA combines transmit signals from different bands. The maximum total power transmitted from a mobile device is not increased in these cases, so for two transmit bands, each band carries half the power of a normal transmission, or 3 dB less than a non-CA signal.
- Because different PAs are used to amplify the signals in different bands, and the transmit power is reduced for each, the PA linearity isn't an issue.
- However, Switches have to deal with high-level signals from different bands that can mix and create intermodulation products. These new signals can interfere with one of the active cellular receivers or even another receiver on the phone, like the GPS receiver. To manage these signals, switches must have very high linearity.

Other considerations for RF?

- Simplify the RF architecture.
- Linearity of RF CA power amplifier.
- Cancellation of interference in CA RF RX.

References

- IEEE papers.
- 3GPP specifications.
- Qualcomm, keysight webpages.
- Larry Miller, “Carrier Aggregation Fundamentals For Dummies” , Qorvo, 2016

Thank You!

Lecture : The Nonlinearity of Power Amplifier

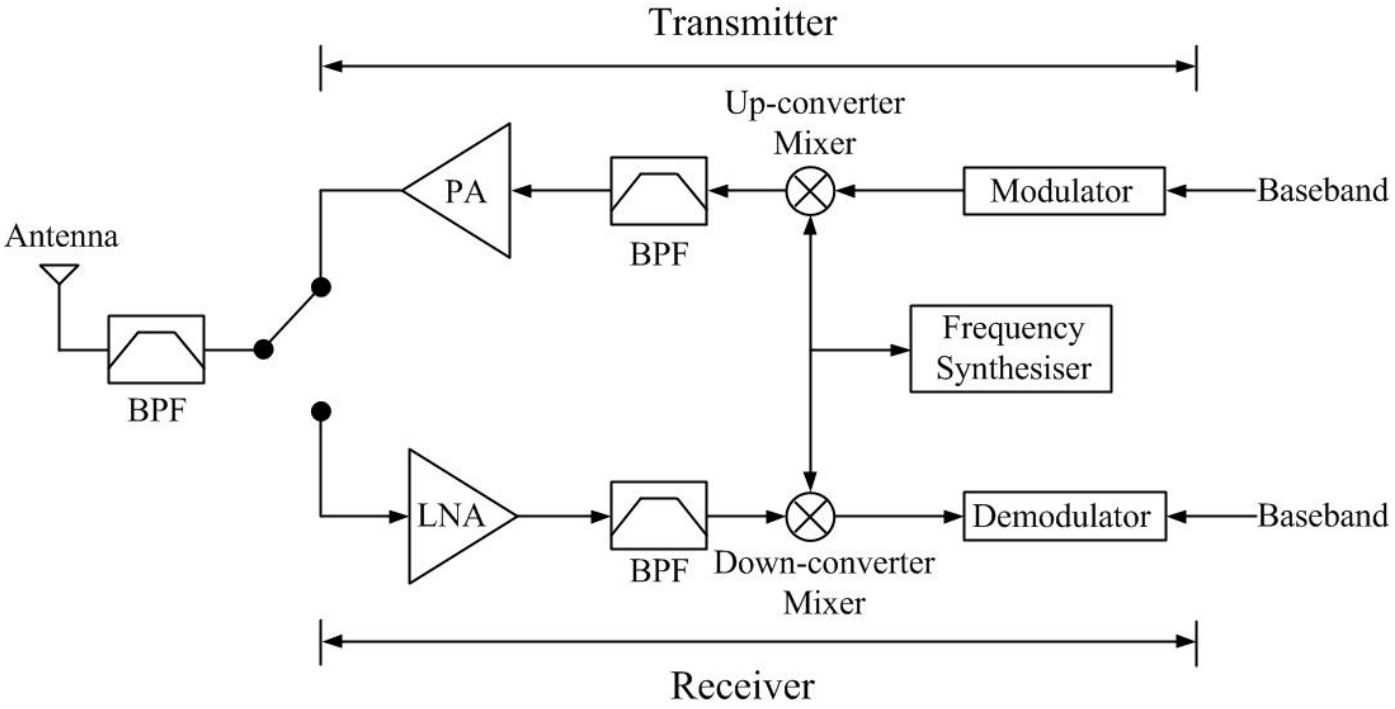
Sen Wang
王紳
Department of Electronic Engineering & Graduate Institute of Computer and Communication Engineering
National Taipei University of Technology
Taipei 106, Taiwan, R.O.C.

Outline

- Introduction
- PA Categories
- Common PA Topology
- Nonlinear Effects

Introduction

Introduction (I)

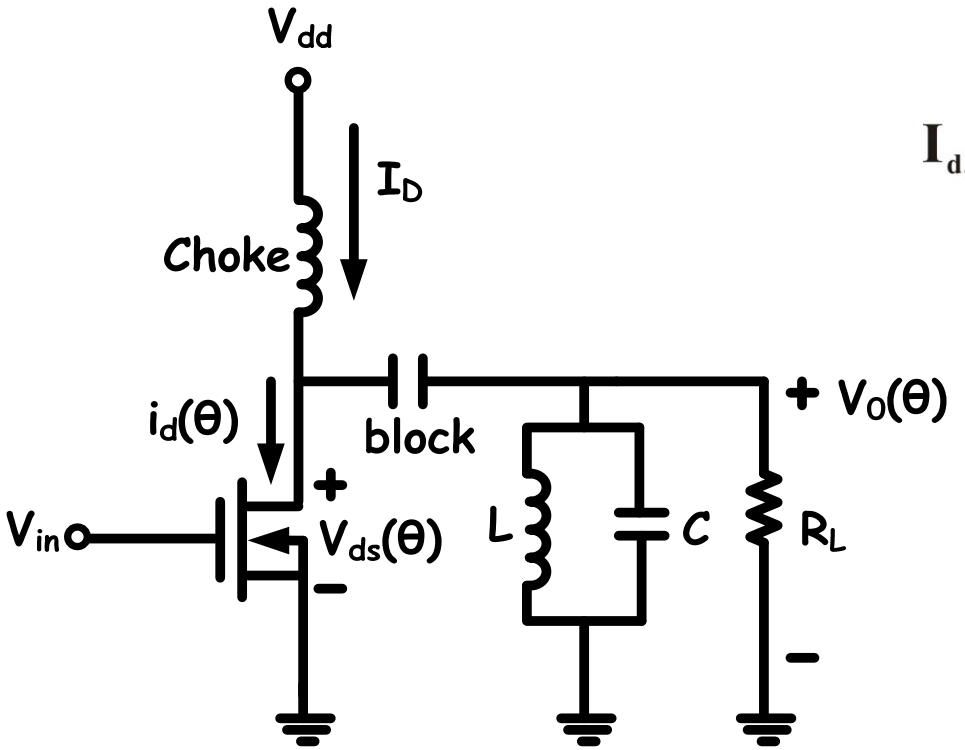


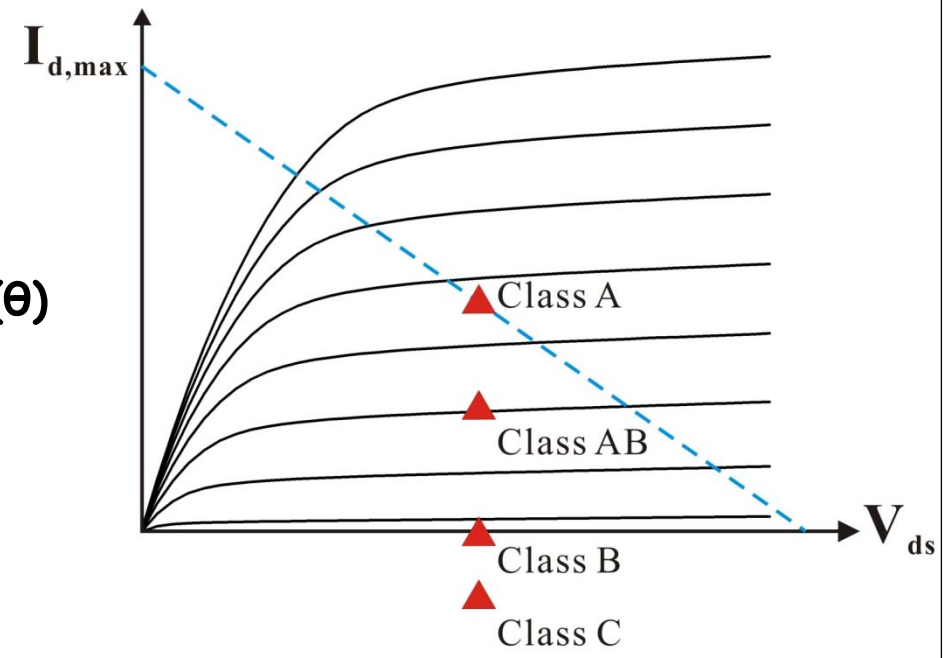
- PAs are used in the final stages of wireless transmitters and request high output power.
- Requiring superior linearity to avoid signal distortions.
- Output power(distance), efficiency(battery) and linearity(digital modulation).

Introduction (II)

- Typical output power(**Handheld celluar:0.3~0.6W**, **Base station:10~100 W**).
- In small-signal amplifiers designs, the input power is small enough that the transistor can be assumed to operate as a linear device. However, for high input power levels, transistors don't behave linearly.
- IC-based PAs typically have limited power supply voltage to **avoid breakdown** and **metal migration limit** for current.
- CMOS PAs suffer low breakdown voltage and less electron mobility, and therefore their power efficiencies are poor compared to GaAs or InP-based PAs.
- Large dissipated power results in **heat** which is a challenging task in design and **packaging**.

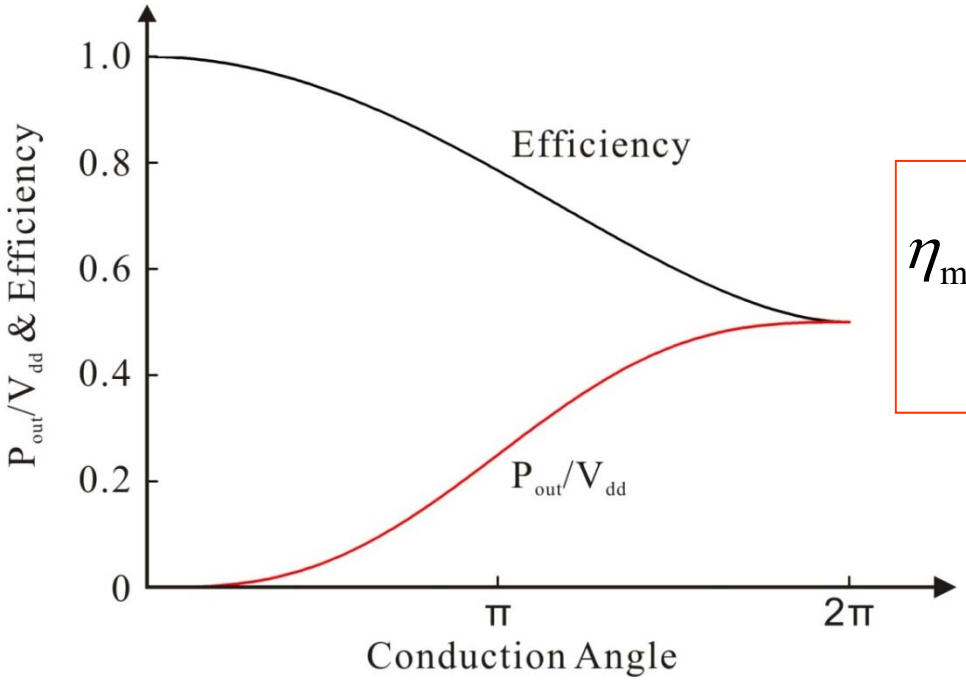
Linear PAs





- PAs are grouped into classes depending **on bias points** and **their voltage and current waveforms**.
- Linear PAs: Class A, B, AB, and C.
- Efficiency and linearity performances.

Output Power and Efficiency



$$\eta_{\max} = \frac{P_{out,\max}}{P_{dc}} = \frac{\theta - \sin\theta}{4(\sin\frac{\theta}{2} - \frac{\theta}{2}\cos\frac{\theta}{2})}$$

- **Conduction angle (θ): The fraction of the full cycle for which current is flowing in the driver transistor.**

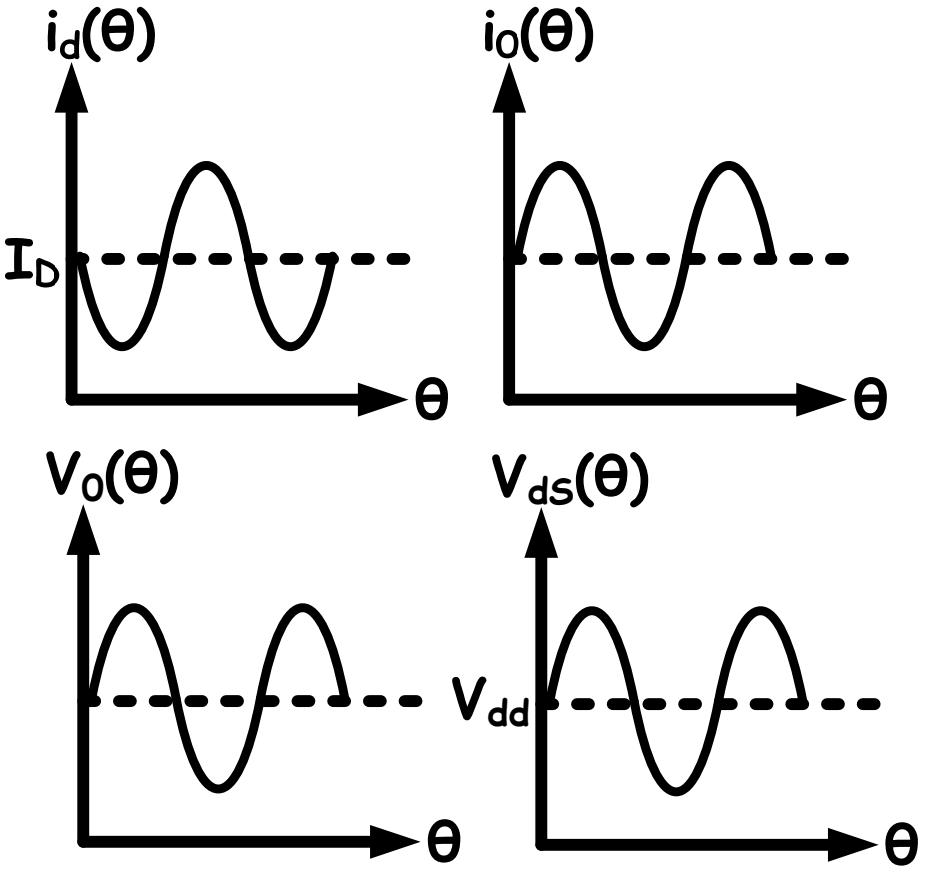
- **Higher conduction angles result in better linearity but lower efficiency.**

Improve Efficiency

- Power losses in transistors must be minimized. Current should be minimum while voltage is high, and vice versa.
- For class B and C, the current is set to zero for part of the cycle where the voltage is high. There is still an overlap of nonzero voltage and current to cause some loss.
- Class D, E, F, and S, use the transistor as a switch to pump a highly resonant tank circuit, and the voltage across the transistor is also nonlinear, leading to higher efficiencies. (up to 100%)
- Class G and H PAs maintain linearity and power a linear amplifier form a variable or switched power supply.

PA Categories

Class A Power Amplifier



$$P_{dc} = V_{dd} I_{dc} = V_{dd}^2 / R$$

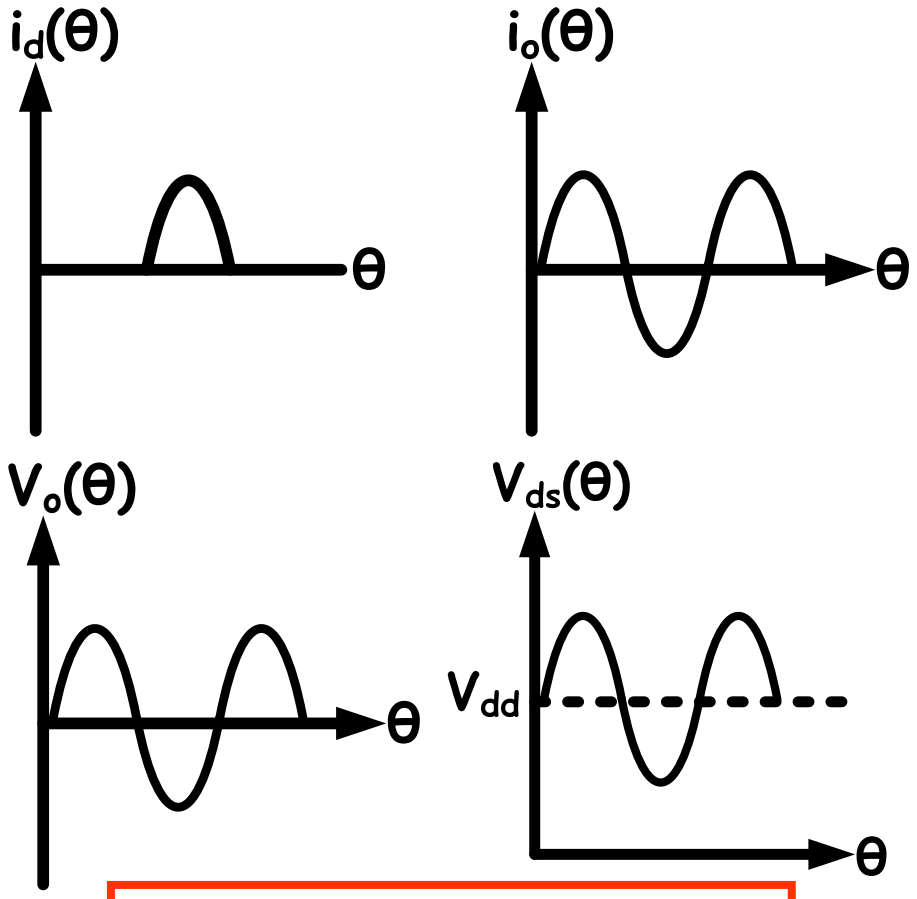
$$P_{out} = V_{rms} I_{rms} = \frac{(V_p/\sqrt{2})^2}{R} = \frac{V_p^2}{2R}$$

$$\eta = \frac{P_{out}}{P_{dc}} = \frac{V_p^2}{2V_{dd}^2} \le \frac{1}{2}$$

- **Most small-signal and LNAs operate as a class A circuit.**
- **In saturation region with 360º conduction angles.**
- **Up to 50% efficiency without considering other losses.**
- **Practical designs featuring less than 30% power efficiency.**

$$\eta_{max} = \frac{2\pi - \sin 2\pi}{4(\sin\pi - \pi\cos\pi)} = \frac{1}{2}$$

Class B Power Amplifier



$$P_{dc} = V_{dd} I_{dc} = \frac{2 V_p V_{dd}}{\pi R}$$

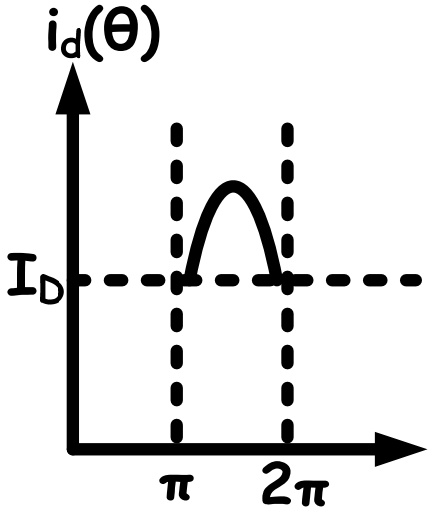
$$P_{out} = V_{rms} I_{rms} = \frac{V_p^2}{2R}$$

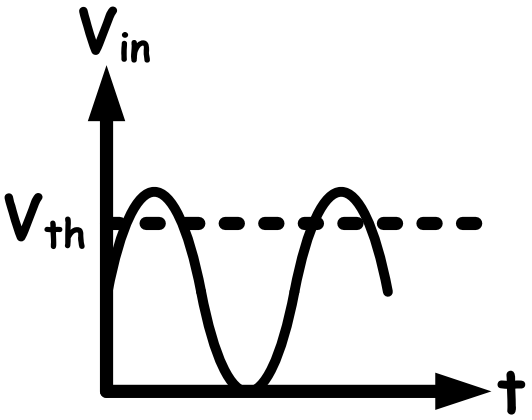
$$\eta = \frac{P_{out}}{P_{dc}} = \frac{\pi V_p}{4 V_{dd}} \le \frac{\pi}{4}$$

$$\eta_{max} = \frac{\pi - \sin\pi}{4(\sin\frac{\pi}{2} - \frac{\pi}{2}\cos\frac{\pi}{2})} = \frac{\pi}{4}$$

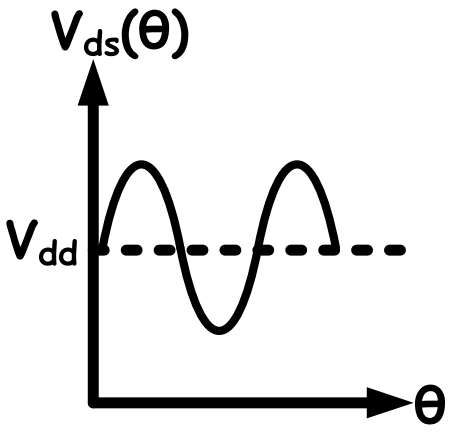
- 180° conduction angles.
- Usually two complementary transistors are operated in this topology to provide amplification over the entire cycle.
- Up to 78% efficiency without considering other losses.

Class C Power Amplifier



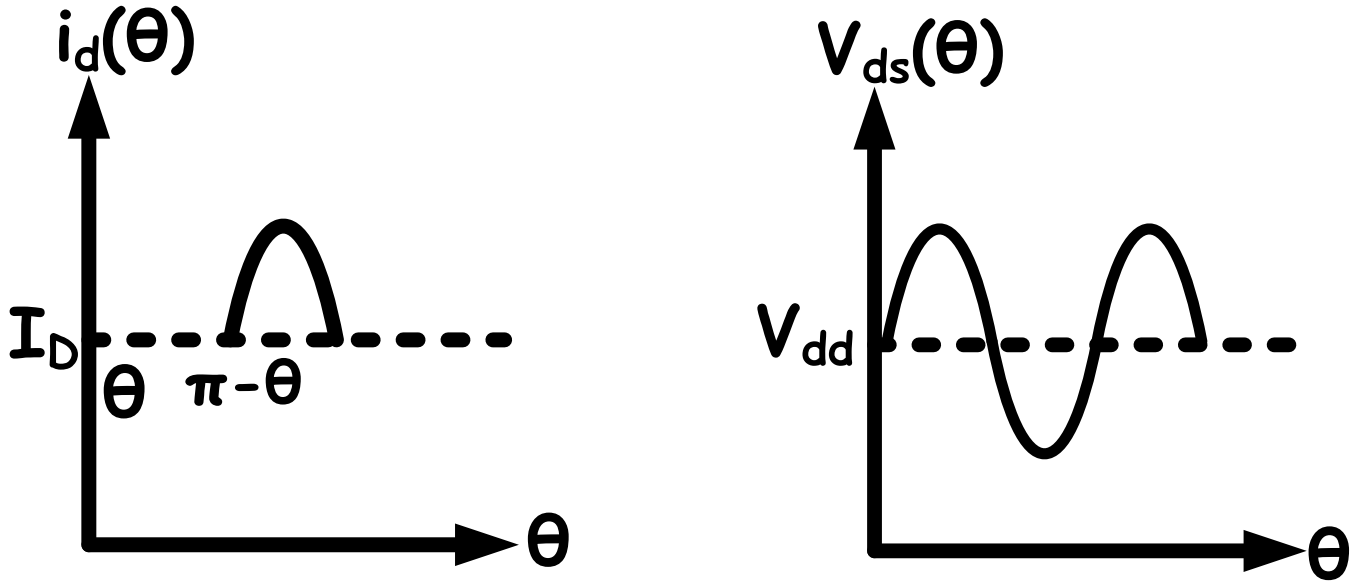


$$\eta = \frac{\theta - \sin\theta}{4\left(\sin\frac{\theta}{2} - \frac{\theta}{2}\cos\frac{\theta}{2}\right)} > \frac{\pi}{4}$$



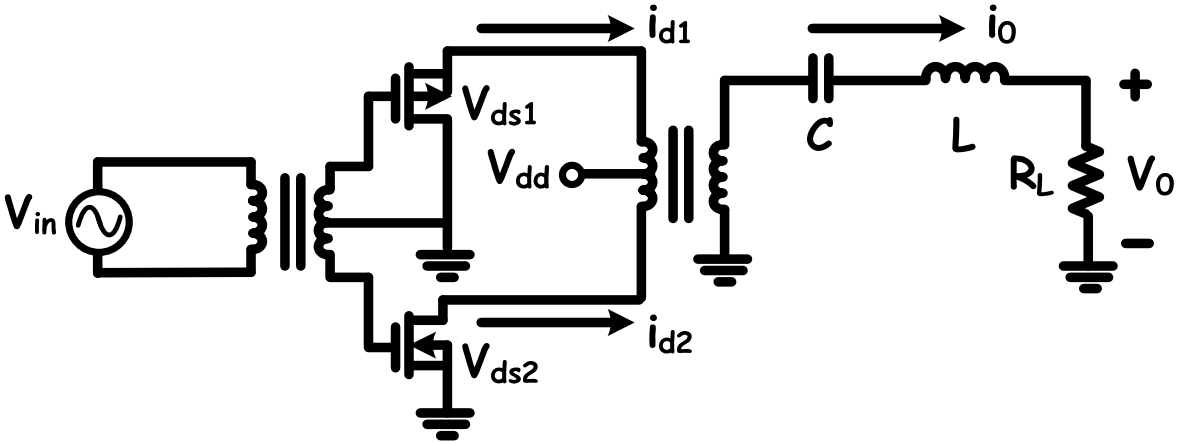
- Less than 180° conduction angles.
- Drive the transistor near cut-off region for more than half of the input signal.
- With a resonant circuit in the output stage to recover the fundamental signals.
- Up to 100% efficiency without considering other losses.

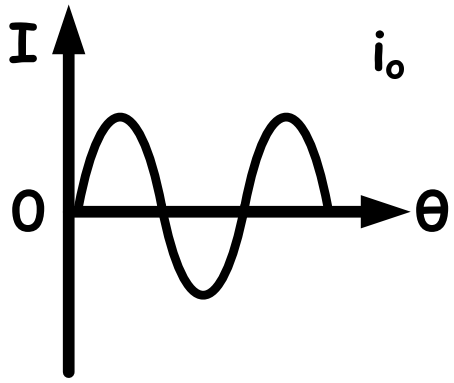
Class AB Power Amplifier

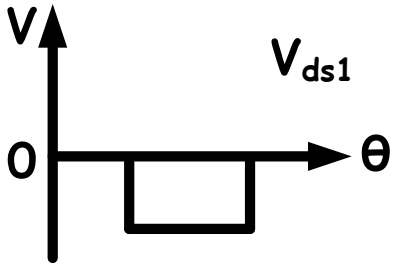


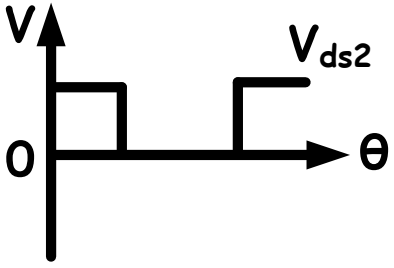
- Operating bias point between Class A and Class B with 180° ~360° conduction angle.
- Linearity and efficiency performances (between Class A and Class B)

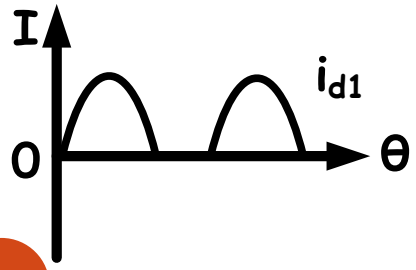
Class D Power Amplifier

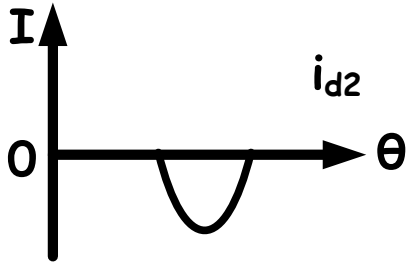










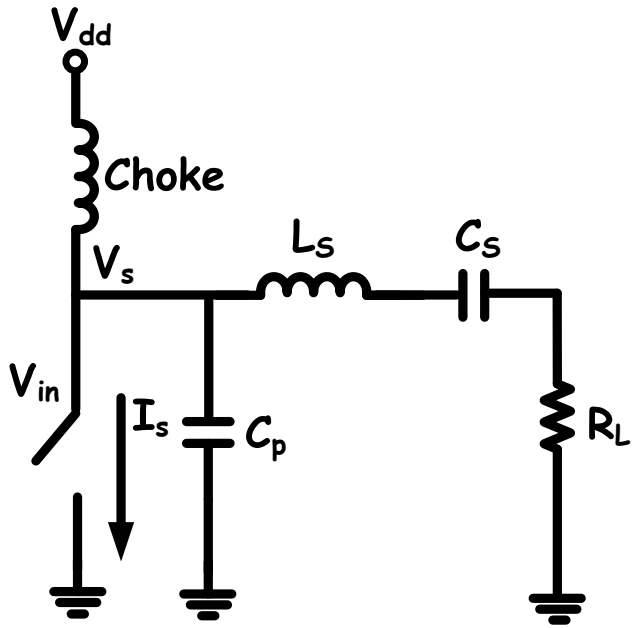


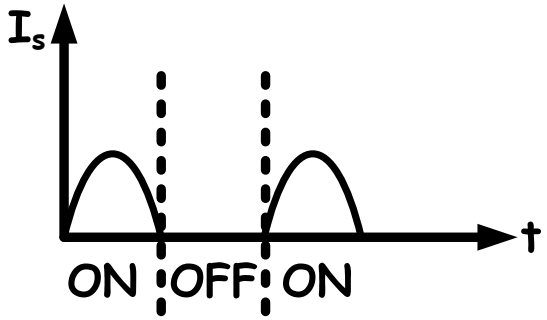
- Switch method (PMOS and NMOS).
- LC filter to eliminate harmonics.
- Ideal efficiency up to 100%.
- Practical designs featuring less than 50% power efficiency (Limited by imperfect square wave and switch speed).

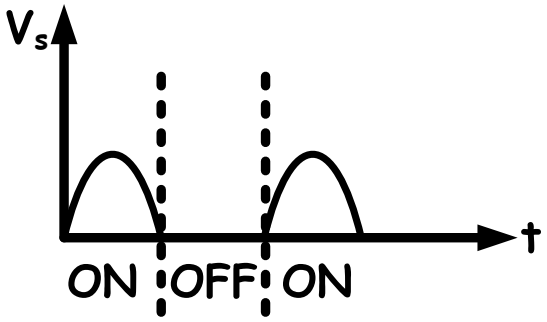
Class E Power Amplifier (I)

Assumption:

- The choke is large (only I_{dc} flows through it).
- Q factors of the output filter is extremely high.
- The transistor behaves as a perfect switch.(When it is on, the Vs is zero, and when it is off the I_{dc} is zero)
- The transistor output capacitance is independent of voltage.





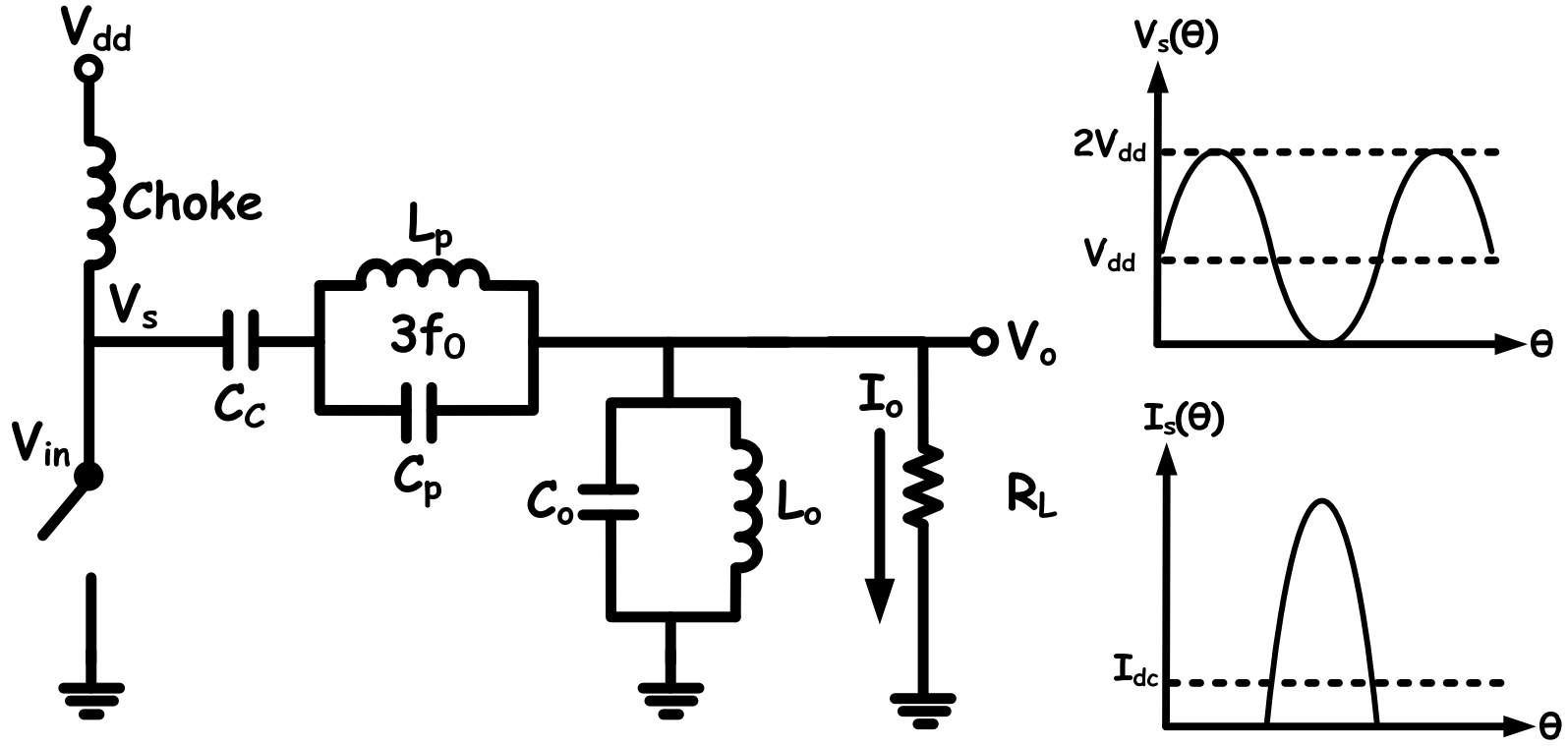


Class E Power Amplifier (II)

- No voltage and current at the same time.
- The Capacitor Cp is the combination of the parasitic transistor output capacitor and an actual added capacitor.
- A capacitor across the output of the transistor is possible to obtain close to 100% efficiency even with parasitics.
- For lossless components, the only loss is due to the discharge of Cp when the switch turns.
- With careful design, 80%-efficiency designs are feasible in practical.

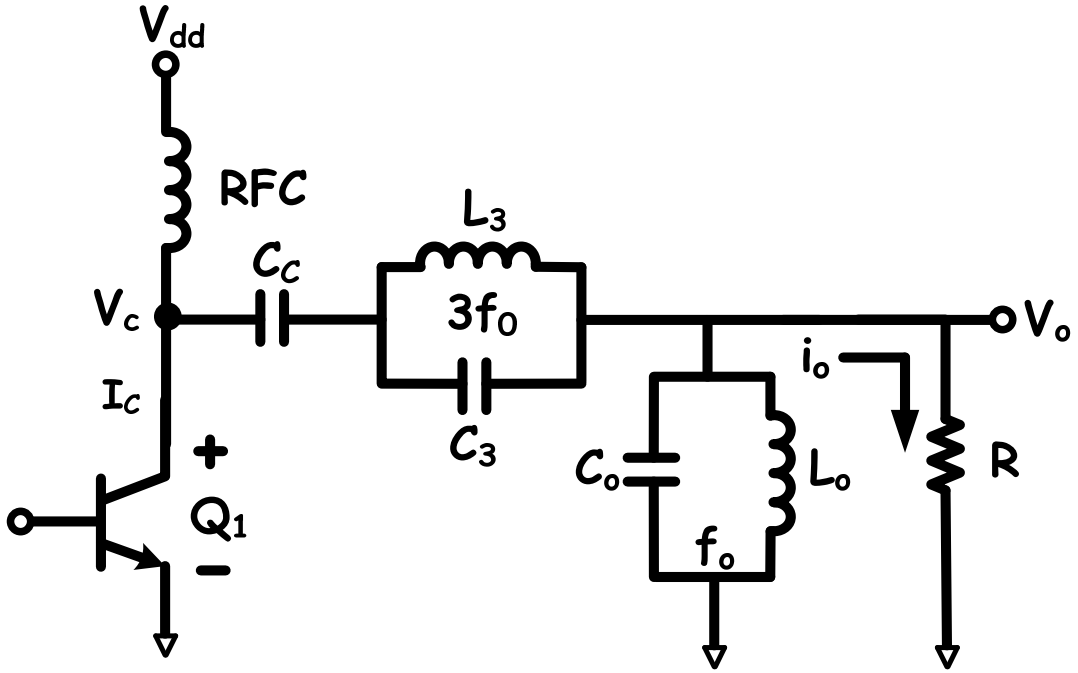
Class F Power Amplifier (I)

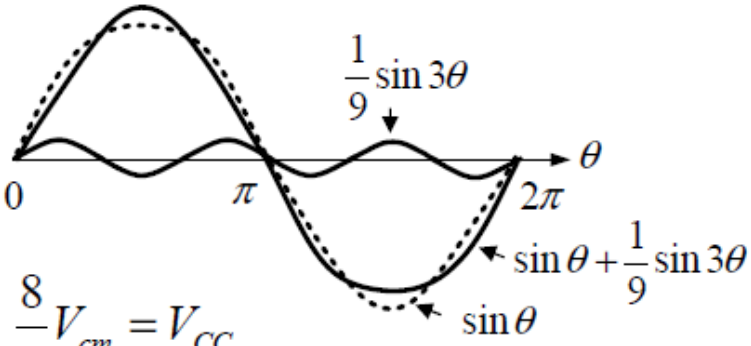
- Additional harmonic is added to the fundamental to produce Vs more like a square wave. This means Vs is lower when Is is flowing, but higher while Is is not flowing.



Class F Power Amplifier (II)

- Lo and Co make sure that the output is sinusoid.
- The Lp and Cp causes a 3rd harmonic component in Vs. The 3rd harmonic component produces a flattening of Vs, which results in higher efficieny and higher output power.





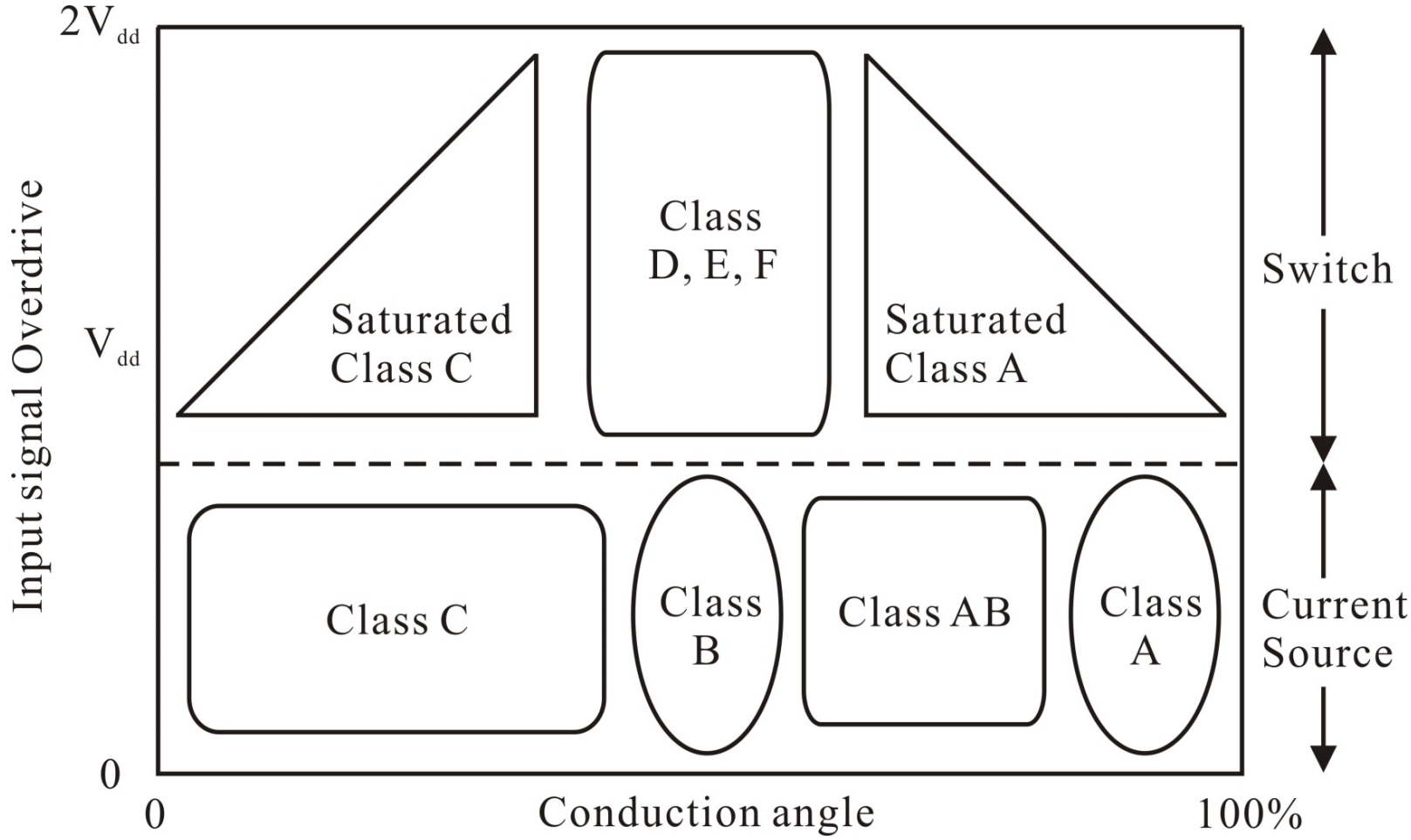
$$\frac{8}{9}V_{cm} = V_{CC}$$

$$\therefore V_{cm} = \frac{9}{8}V_{CC}$$

Comparison (I)

Class	Modes	Conduction Angle	Output Power	Max. Efficiency	Gain	Linearity
A	Current Source	100%	Moderate	50%	Large	Good
B		50%	Moderate	78%	Moderate	Moderate
AB		>50% <100%	Moderate	78-50%	>Class B	Better
C		<50%	Small	100%	Small	Poor
D	Switch	50%	Large	100%	Small	Poor
E		50%	Large	100%	Small	Poor
F		50%	Large	100%	Small	Poor

Comparison (II)

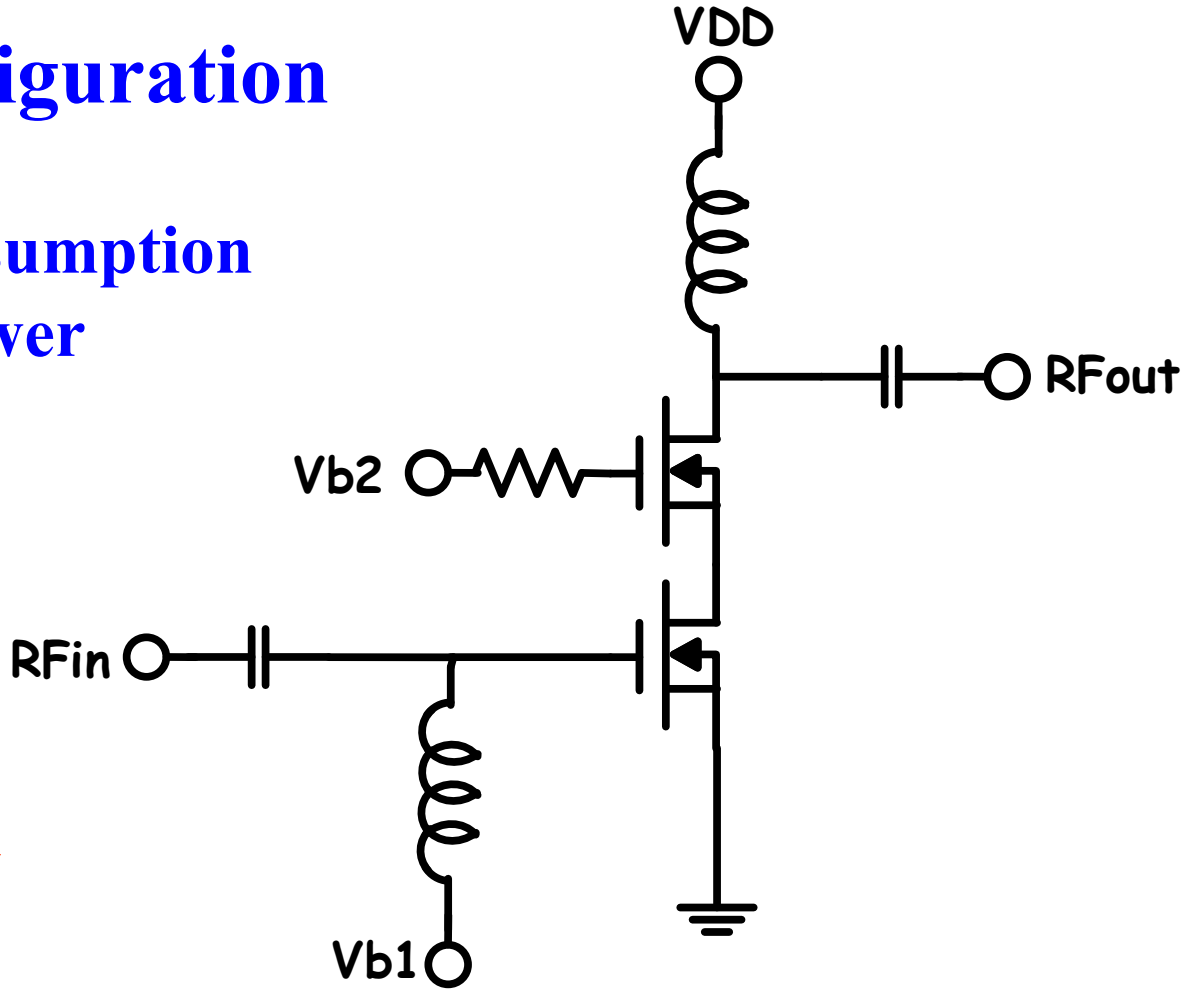


Common PA Topologies

Common PA Topologies (I)

Cascode Configuration

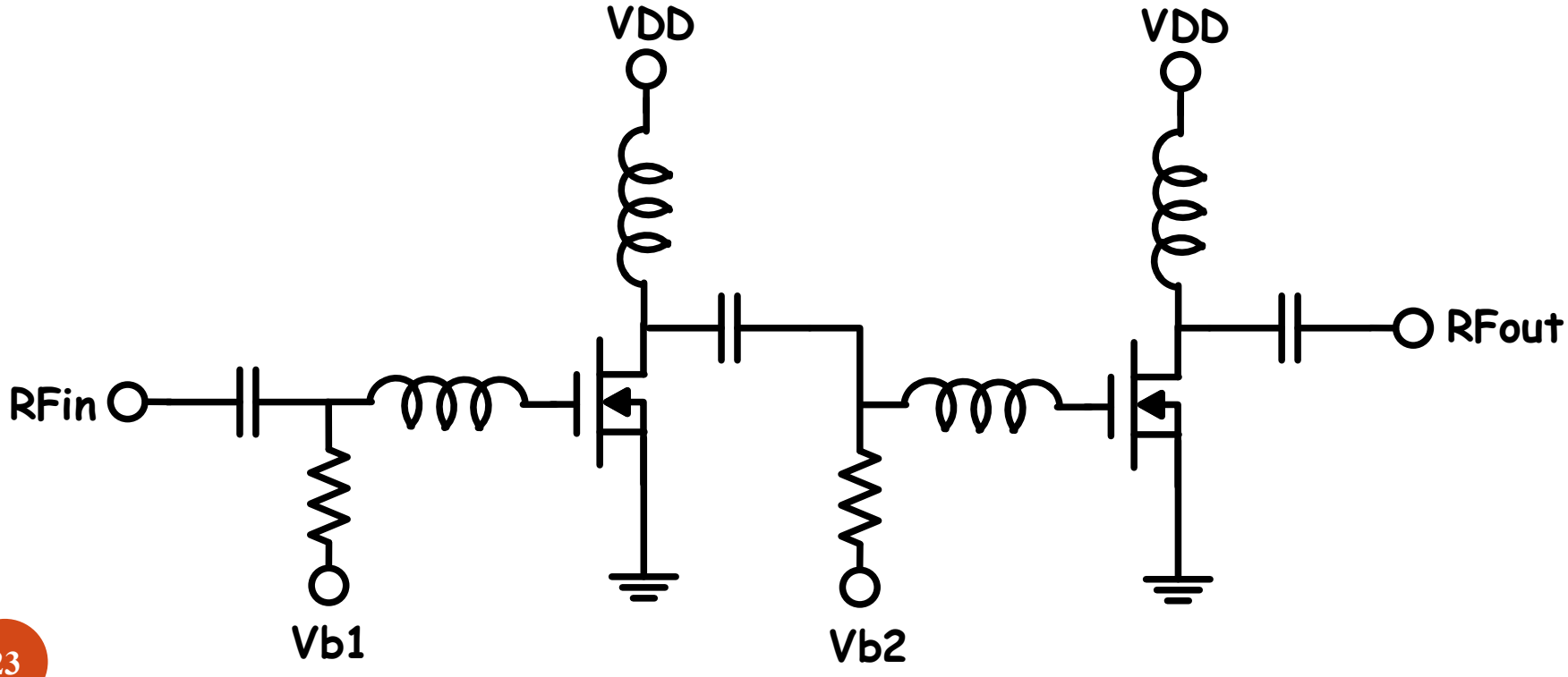
- Advantage
  - Low power consumption
  - High output power
  - High PAE
  - Good linearity
  - Small Area
- Disadvantage
  - Low Power gain



Common PA Topologies (II)

Cascade Configuration

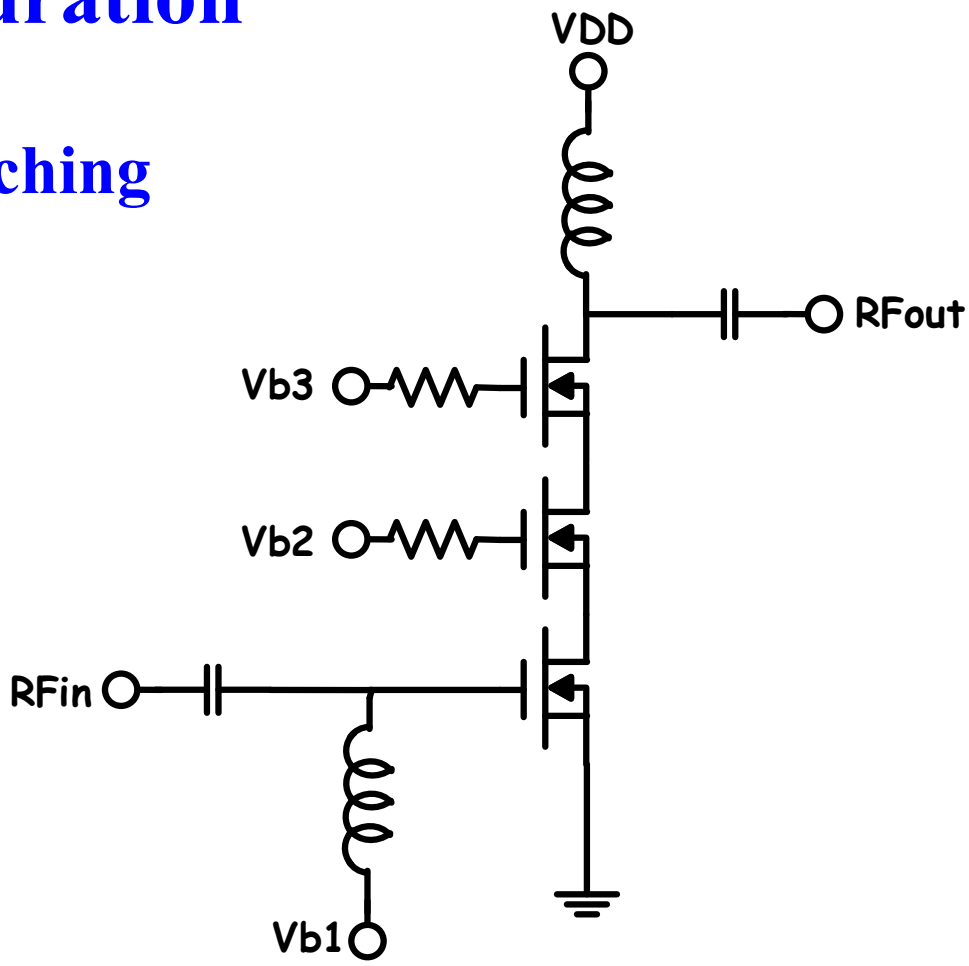
- **Advantage**
  - High Power Gain
  - Low power Consumption
- **Disadvantage**
  - Need inter stage matching
  - Low output power



Common PA Topologies (III)

Multi-Cascode Configuration

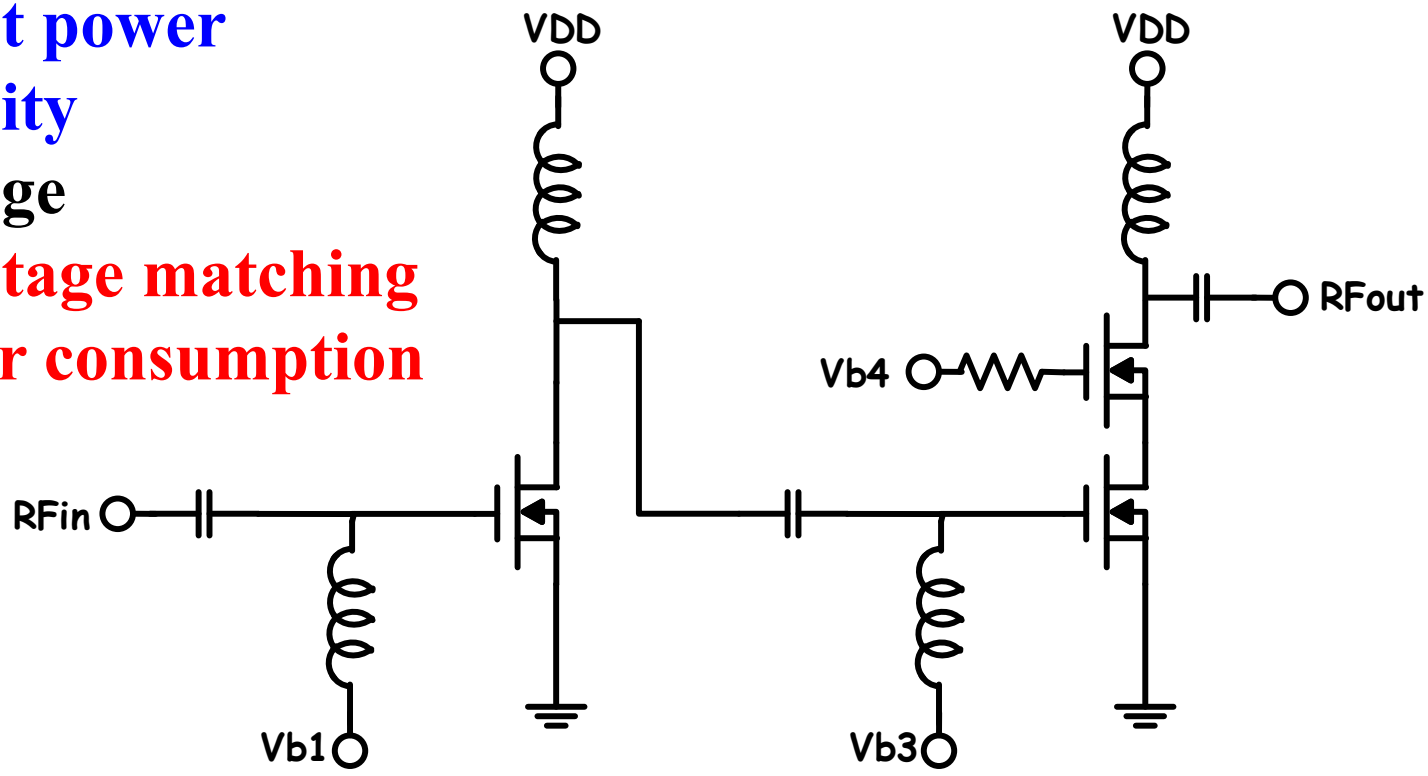
- **Advantage**
  - Don't need inter stage matching
  - Large output power
  - High PAE
  - Good linearity
- **Disadvantage**
  - Low Power gain
  - Large power consumption
  - Low stability



Common PA Topologies (IV)

Cascade with Cascode Configuration

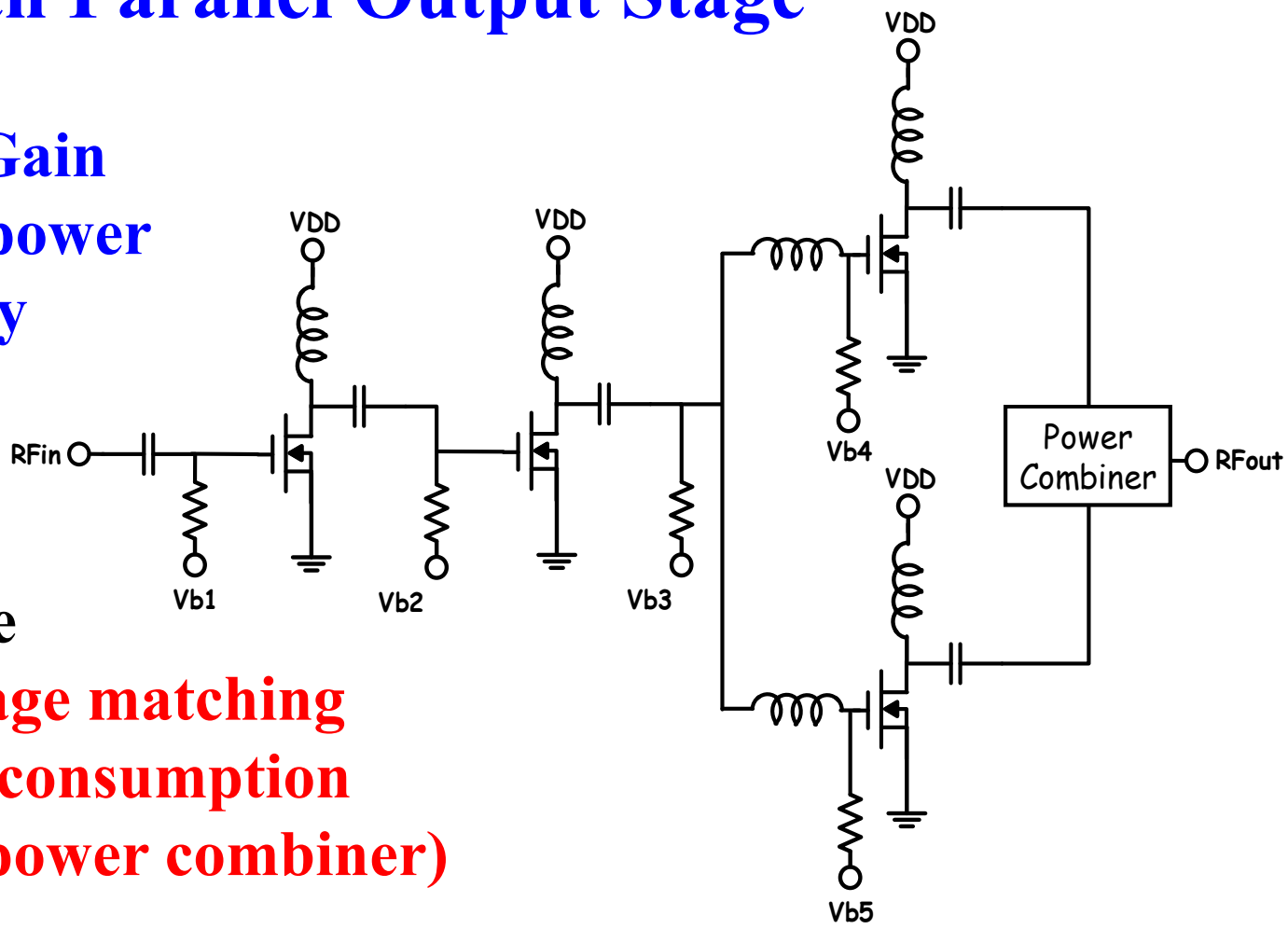
- **Advantage**
  - High Power Gain
  - Good output power
  - Good linearity
- **Disadvantage**
  - Need inter stage matching
  - Large power consumption



Common PA Topologies (V)

Cascade with Parallel Output Stage

- **Advantage**
  - High Power Gain
  - High output power
  - Good linearity
- **Disadvantage**
  - Need inter stage matching
  - Large power consumption
  - Large Area (power combiner)



Nonlinear Effects

Nonlinear Effects

• The distortion of an RF transceiver are resulted from internal interferences and external interferences.

1) The internal interferences are generated from the nonlinear effect of its own devices.

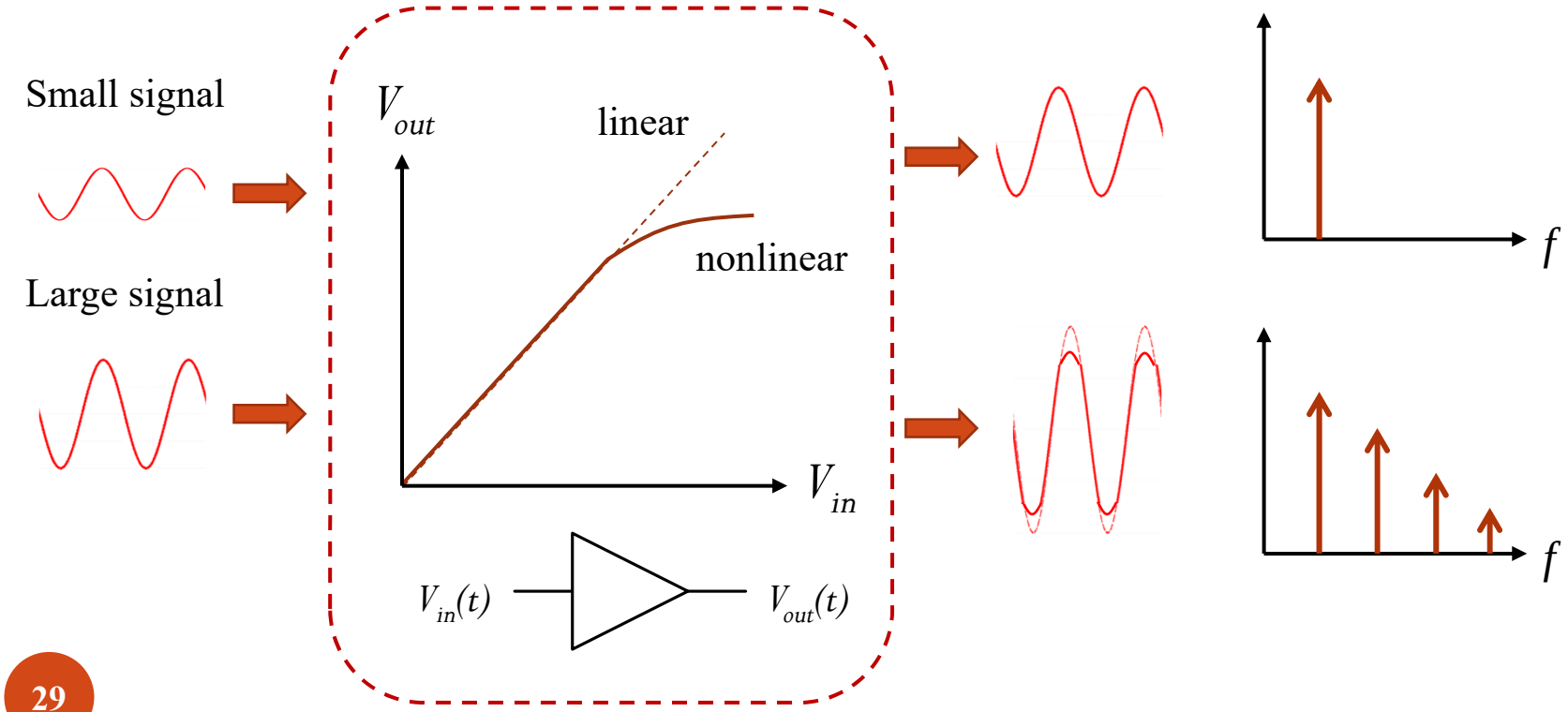
2) The external interference are from outside the transceiver and intercepted by the antenna or EM coupling.

3) Internal distortion is primarily generated from power amplifier

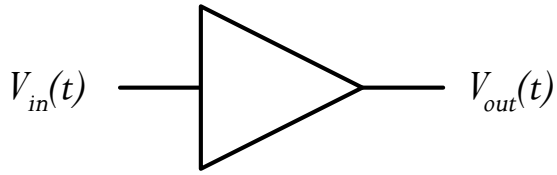
Nonlinear Memoryless Device

- **An input relationship of a nonlinear memoryless device can be represent as :**

$$v_{\text{out}}(t) = \alpha_0 + \alpha_1 v_{\text{in}}(t) + \alpha_2 v_{\text{in}}^2(t) + \alpha_3 v_{\text{in}}^3(t) + \alpha_4 v_{\text{in}}^4(t) + \cdots$$



Nonlinear Memoryless Device (II)

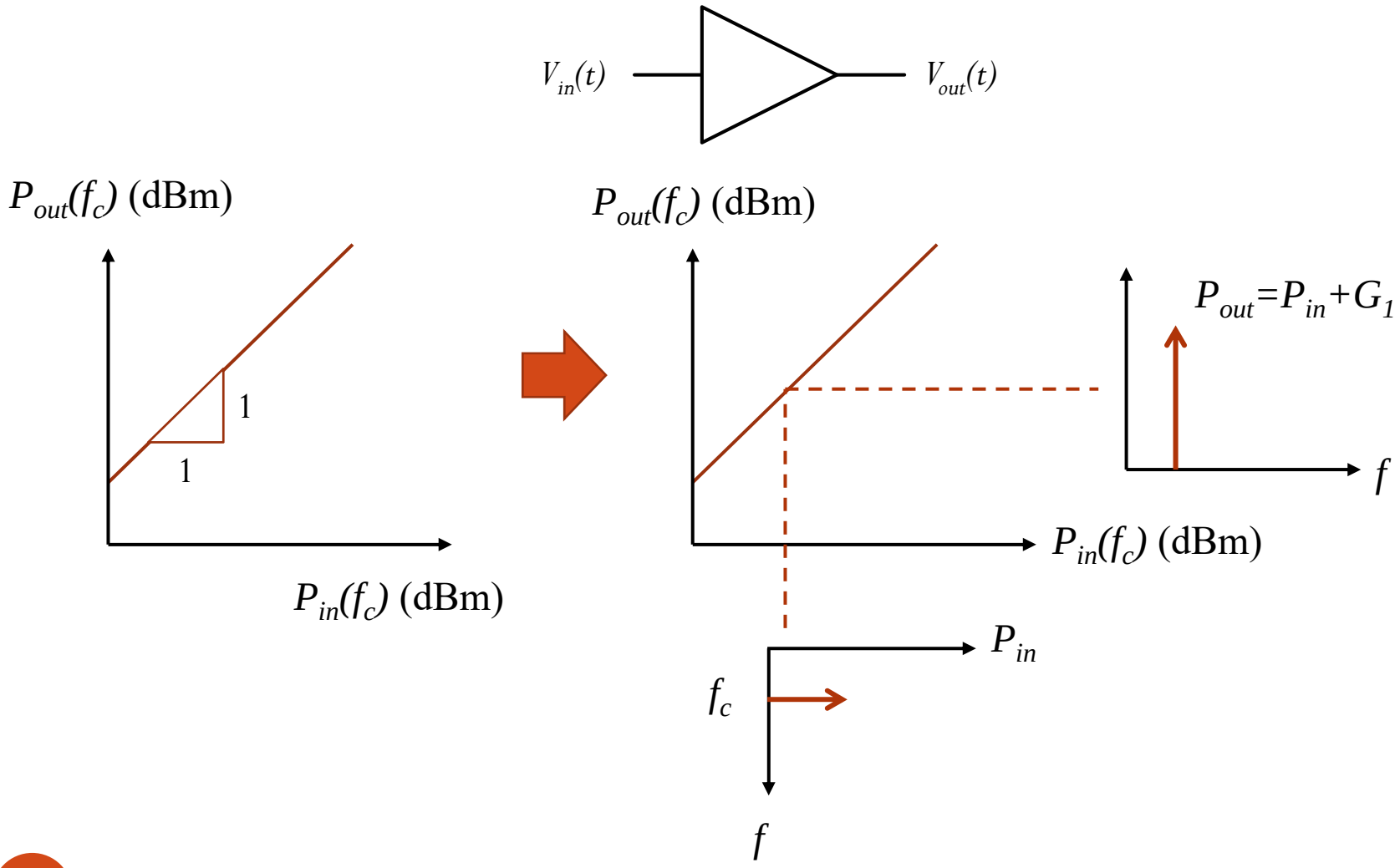


$$v_{\text{out}}(t) = \alpha_0 + \alpha_1 v_{\text{in}}(t) + \alpha_2 v_{\text{in}}^2(t) + \alpha_3 v_{\text{in}}^3(t) + \alpha_4 v_{\text{in}}^4(t) + \cdots$$

Coefficients α_1, are depending on

1) DC bias, RF characteristics of the active device used in the circuit.
2) Magnitude v_{in}, of the signal.
3) When $P < P_{1dB}$ (linear region), all can be treated as constant.

Linear Amplification



Analysis of 1dB-Compression Point (I)

- At P_{1dB}, the output power is compressed 1dB, i.e.,

$$10log\frac{P_{desired+distroted}}{P_{desired}}=20\log\frac{\alpha_1 A_{1dB}+\frac{3}{4}\alpha_3 A_{1dB}^3}{\alpha_1 A_{1dB}}=-1 \quad \Rightarrow \quad \frac{\alpha_1 A_{1dB}+\frac{3}{4}\alpha_3 A_{1dB}^3}{\alpha_1 A_{1dB}}=0.891=10^{\frac{-1}{20}}$$

- The input voltage magnitude at P_{1dB} a $A_{1dB}=\sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|}$

$$IP_{1dB}=10\log\left(\frac{1}{2}\frac{(A_{1dB}^2)}{R_{in}}\right)+30=10\log\left(0.0725\frac{\alpha_1}{R_{in}|\alpha_3|}\right)+30=18.6+10\log\frac{\alpha_1}{|\alpha_3|}\ (\text{dBm})$$

$$OP_{1dB}=10\log\left[\frac{1}{2}\frac{\left(\alpha_1 A_{1dB}+\frac{3}{4}\alpha_3 A_{1dB}^3\right)^2}{R_{out}}\right]+30=10\log\left(\frac{0.0575\alpha_1^3}{R_{in}\alpha_3}\right)+30=17.6+10\log\left(\frac{\alpha_1^3}{R_{out}|\alpha_3|}\right)\ (\text{dBm})$$

$$=17.6+10\log\left(\frac{\alpha_1}{R_{out}|\alpha_3|}\cdot\alpha_1^2\right)=IP_{1dB}+(G_1\text{-}1)\ (\text{dBm})$$

Third order Nonlinear Effect (I)

- **Consider only the first-order and the third-order effect of a nonlinear device, i.e.** $v_{out} = \alpha_1 v_{in} + \alpha_3 v_{in}^3$

- **Single-tone excitation:**
  The input signal contains only a sinusoidal signal *vi*= A cosωt, where its available power can be obtained as $P_{in} = A^2 / (2Z_{in})$

- **In-band and out-of-band distortions**
  The output voltage becomes $v_{out} = \alpha_1 A\cos\omega_1 t + \alpha_3 A^3 \cos^3 \omega_1 t$

$$= \left(\alpha_1 A + \frac{3}{4}\alpha_3 A^3\right)\cos\omega_1 t + \frac{1}{4}\alpha_3 A^3 \cos 3\omega_1 t$$

$$= \left(V_1^{(1)} + V_1^{(3)}\right)\cos\omega_1 t + V_3^{(3)} \cos 3\omega_1 t$$

Desired Signal
linear effect

In-band Distortion
3rd-order effect

Out-of-band Distortion
3rd-order effect
3rd harmonic

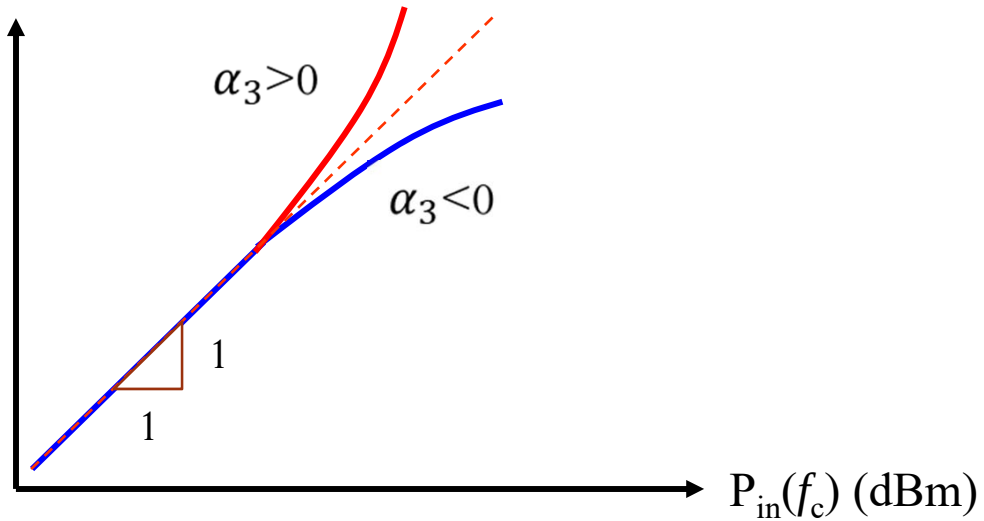
Third order Nonlinear Effect (II)

- **Gain Compression or Enhancement:**

At f_1, the amplified linear-term signal has been mixed with the third-order term

$$v_{out}(f_1) = \left(\alpha_1 A + \frac{3}{4}\alpha_3 A^3\right)\cos\omega t$$

If $a_3 < 0$, the linear gain is compressed, otherwise, it is enhanced



Third order Nonlinear Effect (III)

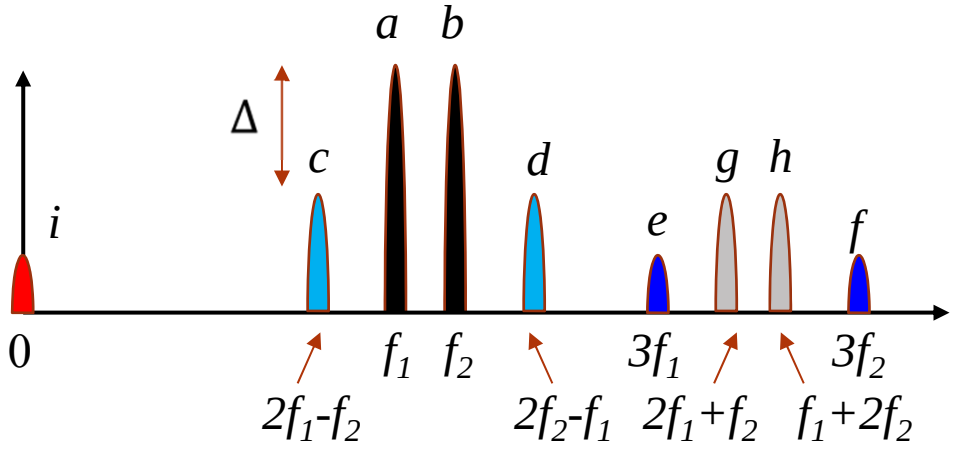
- **Two-tone excitation:** $v_{in}(t) = A\sin\omega_1 t + B\sin\omega_2 t, \omega_1 < \omega_2$

$$v_{out}(t) = \alpha_1 v_{in}(t) + \alpha_3 v_{in}^3(t)$$

$$= \underbrace{\left(\frac{3}{2}\alpha_3 A^2 B + \frac{3}{2}\alpha_3 A B^2\right)}_{i} + \underbrace{\left(\alpha_1 A + \frac{9}{4}\alpha_3 A^3\right)}_{a}\cos\omega_1 t + \underbrace{\left(\alpha_1 B - \frac{9}{4}\alpha_3 B^3\right)}_{b}\cos\omega_2 t$$

$$+ \underbrace{\frac{3}{4}\alpha_3 A^2 B\cos(2\omega_1 - \omega_2)t}_{c} + \underbrace{\frac{3}{4}\alpha_3 A B^2\cos(2\omega_2 - \omega_1)t}_{d} + \underbrace{\frac{1}{4}\alpha_3 A^3\cos 3\omega t}_{e} + \underbrace{\frac{1}{4}\alpha_3 B^3\cos 3\omega_2 t}_{f}$$

$$+ \underbrace{\frac{3}{4}\alpha_3 A^2 B\cos(2\omega_1 + \omega_2)t}_{g} + \underbrace{\frac{3}{4}\alpha_3 A B^2\cos(\omega_1 + 2\omega_2)t}_{h}$$



$$\text{IMR}_{2tone} = \Delta = 2(\text{IP3} - P_{in}) = 2(\text{OIP3} - \text{Pout})$$

a, b: linear term(desired signal) +inband distortion

c, d: IM3, adjacent band distortion

e, f :3rd harmonic

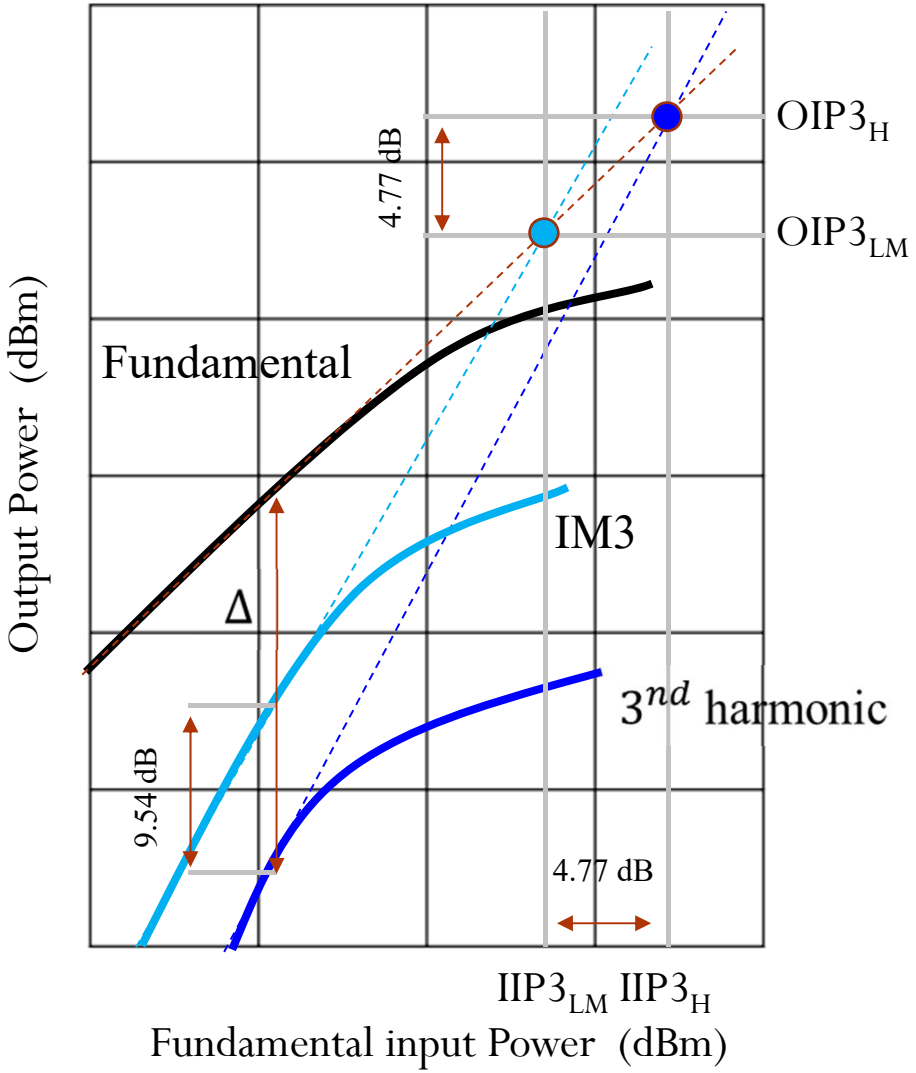
g, h : out of band distortion

i: DC term

Third order Intercept Point

- The slopes for the 3rd-order products are steeper than 2nd-order products since they represent cubic nonlinearities rather than squares. IMs and harmonics change 3 dB for each dB change in the inputs and fundamental outputs.
- Since the slopes of the straight lines are known, these crossing points, called intercept points (IPs), define the 3rd-order products at low levels.
- Intermodulation Ratio (IMR)

$$\begin{aligned} \text{IMR}_{2-\text{tore}} &= \Delta(\text{dB}) = 2\left(MP3 - P_{\text{in}}\right) \\ &= 2\left(OIP3 - P_{\text{out}}\right) \end{aligned}$$



Summary

- Various kinds of power amplifiers were introduced, including the Class A, AB, B, and C linear amplifiers as well as Class D, E, and F nonlinear amplifiers.
- Linear amplifiers have good linearity but poor efficiency on the contrary, the nonlinear amplifiers have very good efficiency but poor linearity.
- The nonlinearities will result in harmonics and intermodulation distortions in frequency domain. And the distortion can be easily defined using frequency-domain parameters related to signal power.
- The nonlinearities can be described by P1dB and intercept points.

Reference

- https://simeneer.blogspot.tw/p/blog-page_4.html. (李健榮 教授-RF Transceiver Module Design/ Multiband RF Transceiver System課程教材)
- RF Microelectronics, Prentice-Hall. Behzad Razavi.
  (代理商: 新月書局)
- Microwave Transistor Amplifiers: Analysis and Design.
  (代理商:高立圖書)
- RF Power Amplifier Design. (張盛富 教授)

Lecture : Linearity Improving and Power Combining Techniques

Sen Wang

王紳

Department of Electronic Engineering & Graduate Institute of Computer and Communication Engineering

National Taipei University of Technology

Taipei 106, Taiwan, R.O.C.

Outline

- Amplifier Linearized Techniques
- Power Combine Techniques

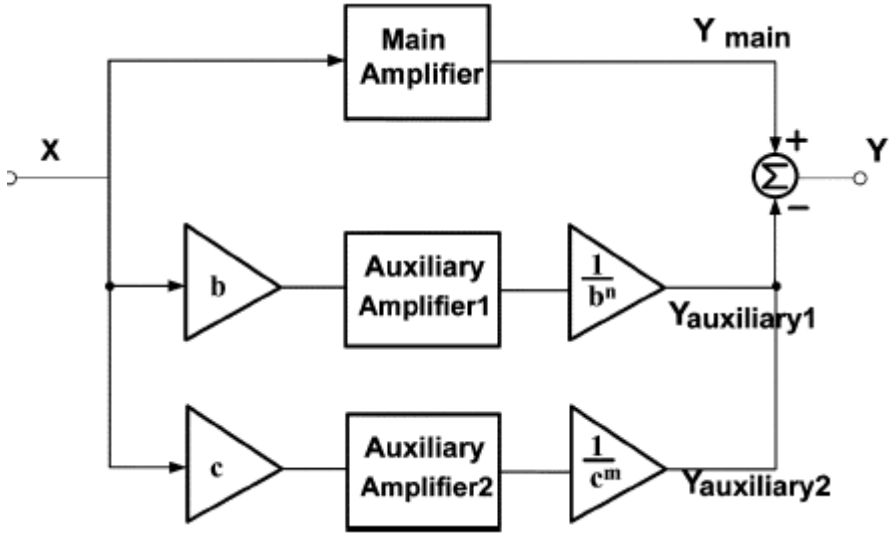
Amplifier
Linearized Techniques

Ref. Chongcheawchamnan, et. al, ”A 900 MHz 16-QAM direct carrier modulation transmitter using feedforward linearization,” *IEEE MTT-S Int. Microwave Symp. Digest*, vol. 3, pp.1495-1498, 2000.

Ref. J. L. Dawson and T. Lee, “Automatic phase alignment for a fully integratedcartesian feedback power amplifier system,” *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2269–2279, Dec. 2003.

Ref. Wei-Tsung Li, et. al, "Parasitic-Insensitive Linearization Methods for 60-GHz 90-nm CMOS LNAs," *IEEE Trans. Microw. Theory Tech*. vol. 60 no. 8 pp.2512-2523, Aug. 2012.

Feed-Forward Technique



1. Phase Shifters and Attenuators are required.
2. Sensitive to Process Variation
3. Large Power Consumption

$$Y_{auxiliary1} = \left[g_1(bX) + g_2(bX)^2 + g_3(bX)^3\right]\frac{1}{b^n}$$

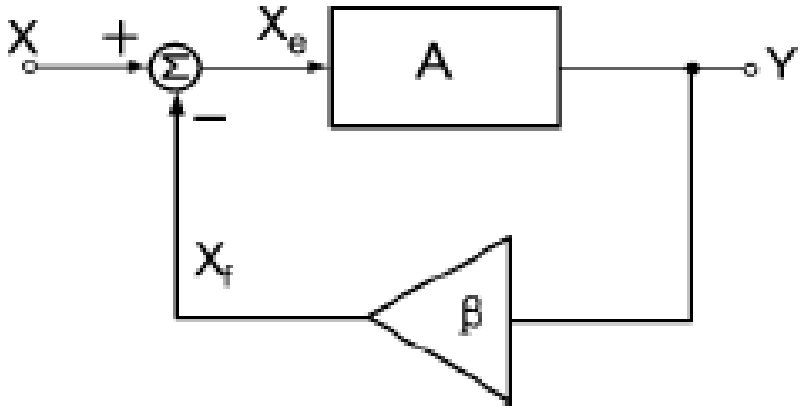
$$Y_{auxiliary2} = \left[g_1(cX) + g_2(cX)^2 + g_3(cX)^3\right]\frac{1}{c^m}$$

$$Y = Y_{main} - Y_{auxiliary1} - Y_{auxiliary2}$$

Nonlinearity Cancellation

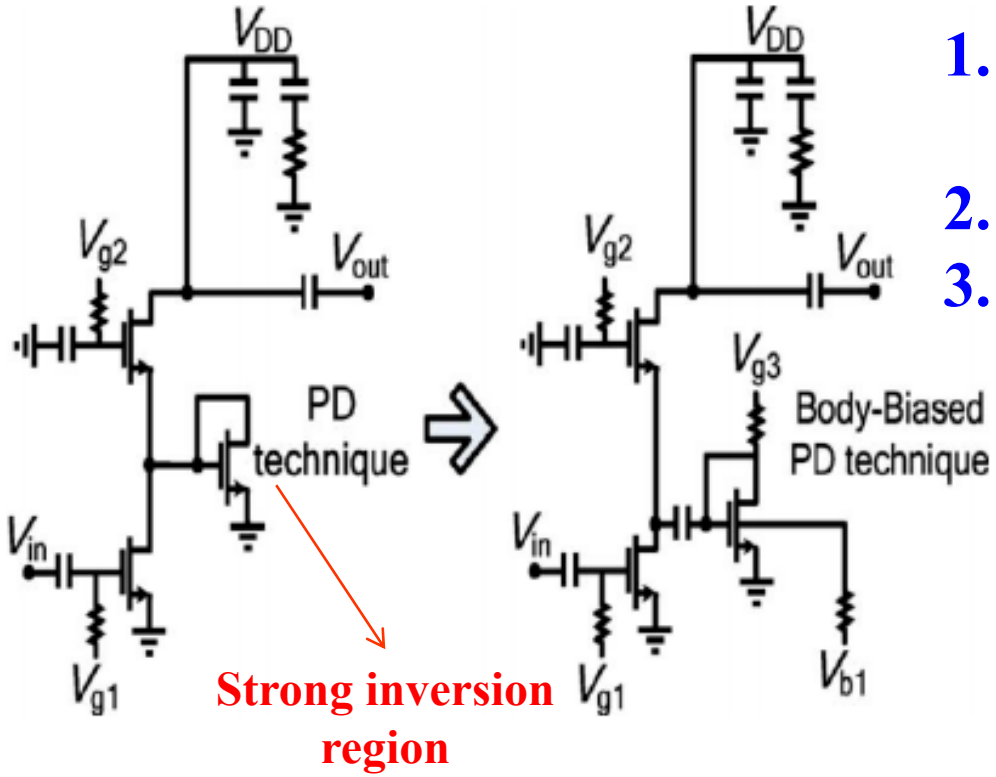
$$= g_1\left(1 - \frac{1}{b^{n-1}} - \frac{1}{c^{m-1}}\right)X + g_2\left(1 - \frac{1}{b^{n-2}} - \frac{1}{c^{m-2}}\right)X^2 + g_3\left(1 - \frac{1}{b^{n-3}} - \frac{1}{c^{m-3}}\right)X^3$$

Feedback Technique



1. **Precise Nonlinearity Cancellation (Analog Feedback)**
2. **Not Sensitive to Process Variation**
3. **Circuit Complexity**

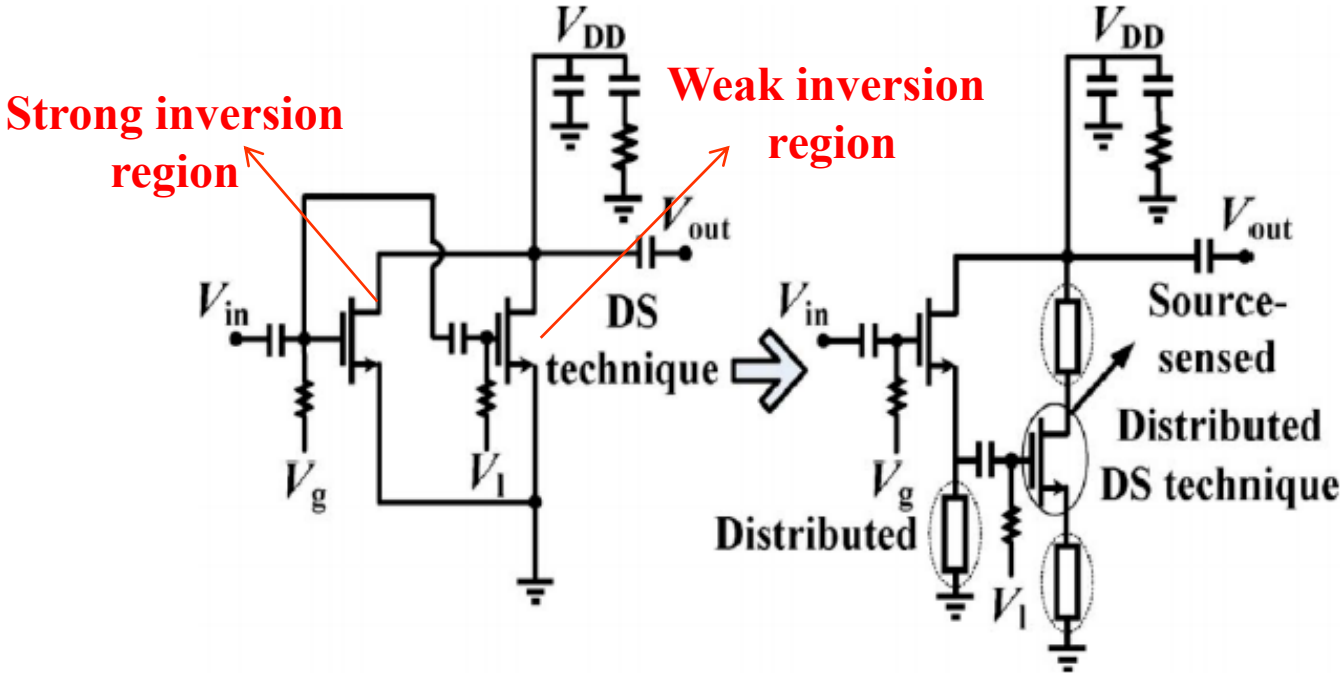
Post-Distortion Technique



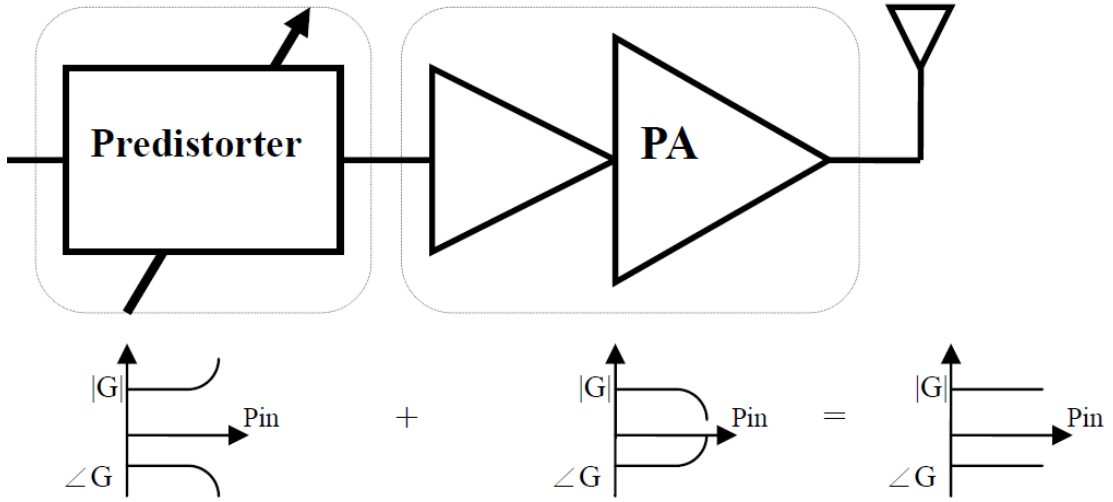
1. Auxiliary transistor in strong inversion region at output
2. Body bias
3. Suitable for integration

Derivative Superposition

1. Main path: Strong inversion region
2. Secondary path: Weak inversion region
3. Distributed DS for Lowering Parasitics Effect



Pre-Distortion Technique



1. **Pre-distorter : To generate AM-AM、AM-PM opposite to the PA**
2. **Achieving Gain Expansion**

Comparison

Technique	Cancellation	Bandwidth	PAE	Size
Feedforward	Good	Wide	Low	Large
Feedback	Good	Narrow	Medium	Medium
Pre/Post Distortion	Medium	Medium	High	Small

Amplifier
Power Combine Techniques

Ref. C.-W. Kuo, H.-K. Chiou, and H.-Y. Chung, "An 18 to 33 GHz fullyintegrated Darlington power amplifier with Guanella-type transmissionline transformers in 0.18 μm CMOS technology," IEEE Microw. Wireless Compon. Lett., vol. 23, no. 12, pp. 668–670, Dec. 2013.

Ref. P. Huang, J. Juo, Z. Tsai, K. Lin, and H. Wang, "A 22-dBm 24-GHz power amplifier using 0.18-μm CMOS technology," in IEEE MTT-S Int. Dig., May 2010, pp. 248–251.

Ref. T.-Y. Huang, Y.-H. Lin, and H. Wang, "A K-band adaptive-bias power amplifier with enhanced linearizer using 0.18-μm CMOS process," in IEEE MTT-S Int. Dig., May 2015, pp. 1–3.

Power Combine Technique(1)

1. Since the single-transistor PA unit in the various semiconductor technologies have limited output power with reasonable power gain and efficiency.

2. To further achieve the high output power and linearity, power combining techniques using power combiner are adopted.

3. The power combining techniques combine the output power of several single-transistor PA units to achieve larger output power. Three important power combination schemes, Wilkinson combiner, balanced amplifier, and transformer combiner, will be discussed.

Power Combine Technique(2)

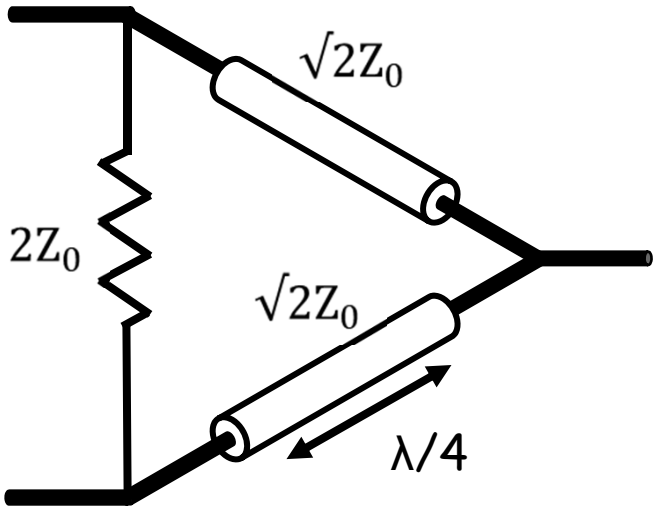
1. The monolithic power combiners can be categorized as 50-Ω matched combiners (e.g. Wilkinson and 90-degree coupler) and non-50Ω matched ones (e.g. transformers).

2. In terms of 50-Ω matched combiner, it is easy to be implemented, but the matching networks for 50-Ω consume a larger chip area.

3. On the other hand, the non-50Ω matched power combiners have the advantage to achieve the power combining and impedance transformation simultaneously in a compact size.

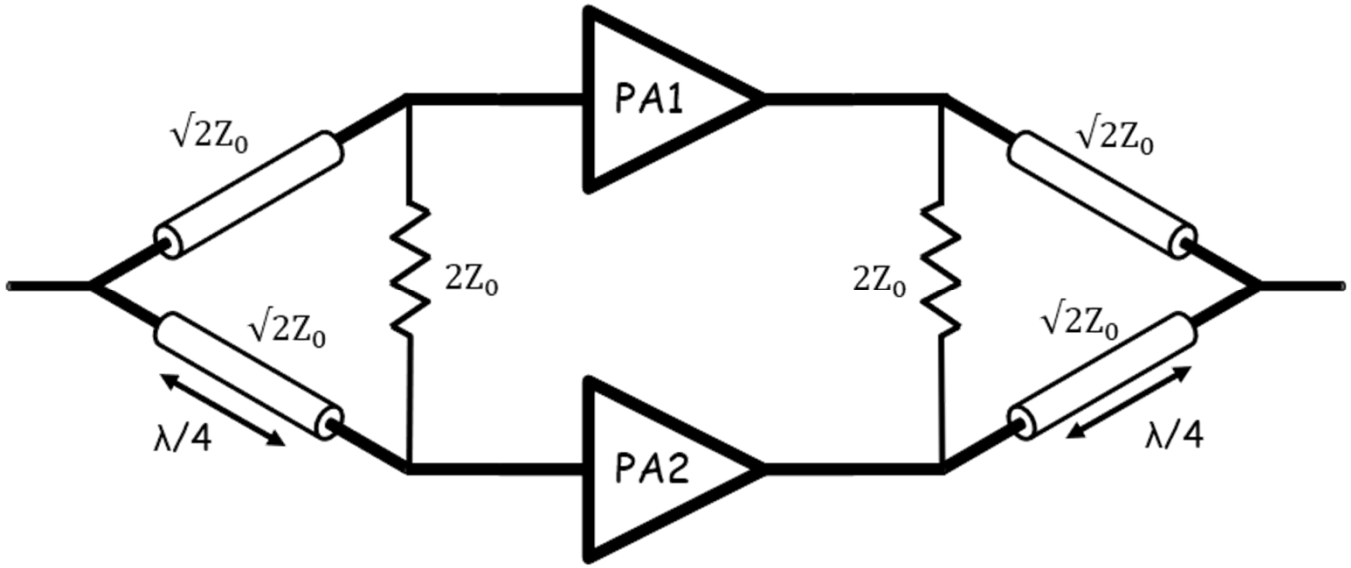
4. Nevertheless, the design of those combiners suffers more challenges such as impedance restriction and complicated power splitting networks.

Power Combine Technique(3)



The Wilkinson power combiner has several advantages such as easy implementation, good port-to-port isolation, and low insertion loss. It can also be a power divider for in-phase power combining techniques.

Power Combine Technique(4)



1.In this figure, Wilkinson power divider splits input power of the PA equally in-phase into two single-transistor PA units for amplification.

2.Two amplified signals at output ports of two single-transistor PA units are combined by a Wilkinson power combiner and double output power can be achieved.

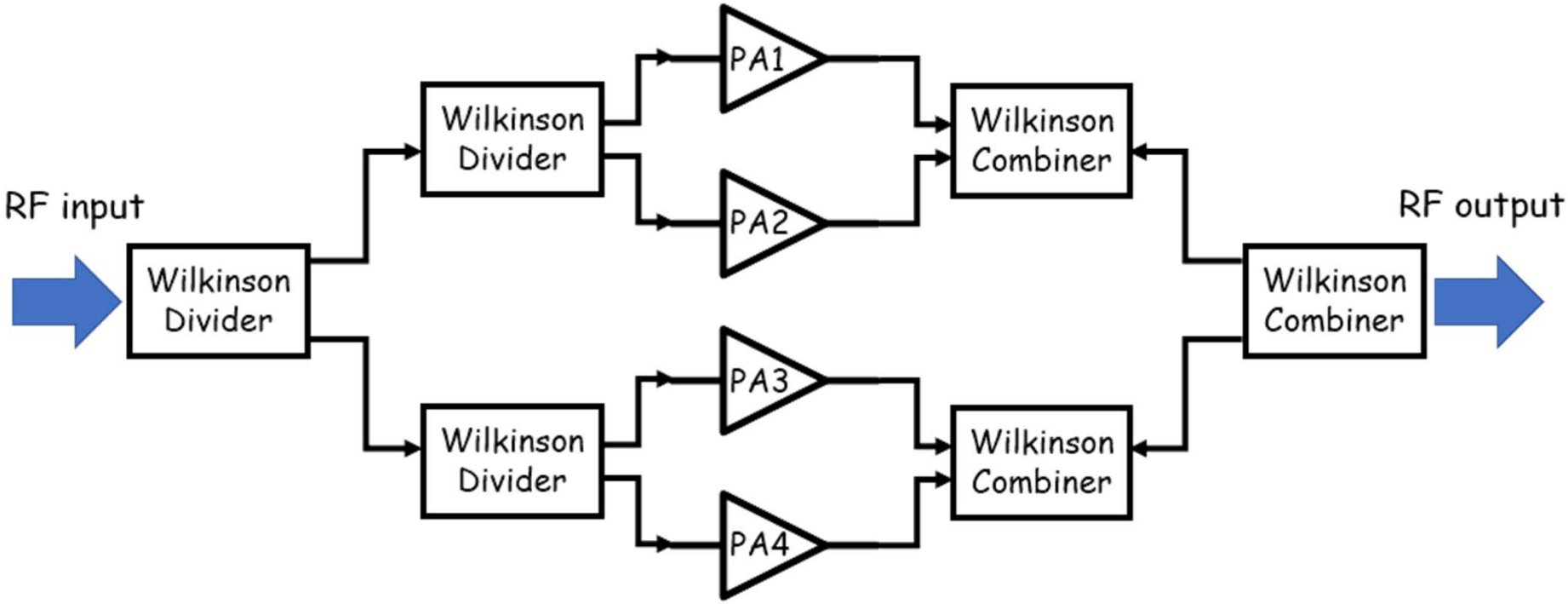
Power Combine Technique(5)

1.In next figure is an example of a four single-transistor PA units in-phase combination PA using cascaded two-way Wilkinson power combiners/dividers for quadruple output power.

2.The input signal of the PA is split equally in-phase into four identical single-transistor PA units by cascaded two-way Wilkinson power dividers. Finally, the four amplified signals are combined by a set of cascaded Wilkinson power combiners (three two-way Wilkinson power combiners) and quadruple output power can be obtained.

3.In addition, the insertion loss of the Wilkinson power combiner may decrease the final combined output power of the whole PA.

Power Combine Technique(6)



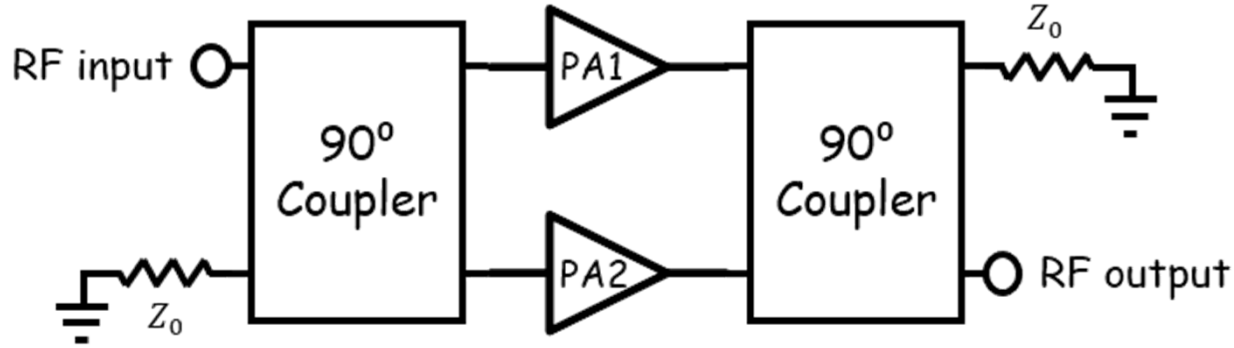
Power Combine Technique(7)

1.The next figure illustrates the balanced amplifier configuration which adopts two identical PA units and two 90 degree 3-dB hybrid couplers.

2.A 90 degree 3-dB hybrid coupler produces two equal-amplitude and quadrature-phase signals from input power of the PA. The two signals are fed into two identical PA units for amplification.

3.Two amplified signals at each output ports of two PA units are recombined by means of the same 90 degree 3-dB hybrid coupler. It should be noted that the connected ports of couplers in the input and output terminals, respectively, need to be exchanged for in-phase combine.

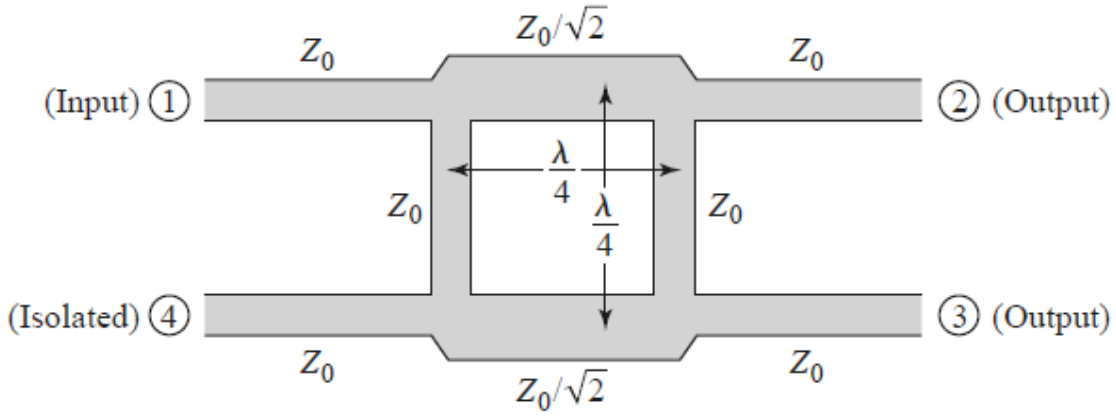
Power Combine Technique (8)



1.The balanced amplifier configuration with 90˚couplers can absorb reflections and improve input/output matching, so the individual PA units can be optimized for output power and gain flatness.

2.In addition, the balanced configuration provides high stability over a wide bandwidth, and it is easy to cascade with another driver stage because of isolation from couplers.

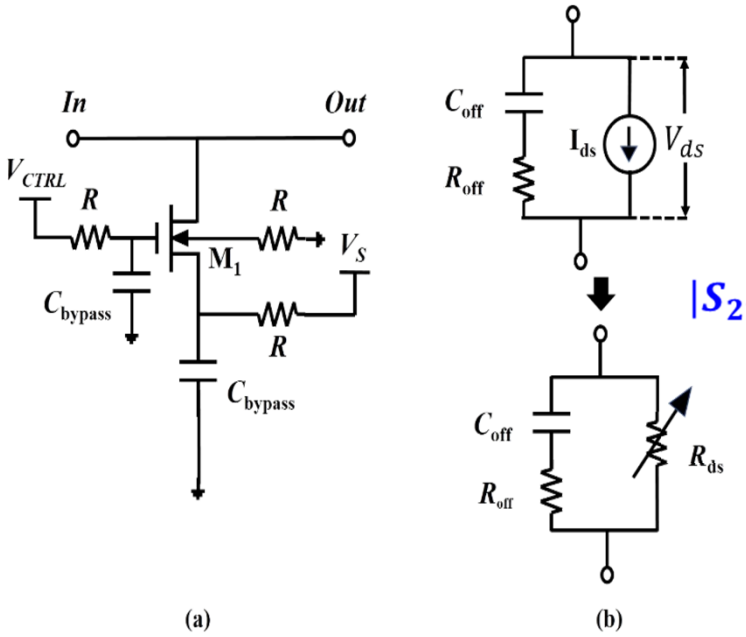
Power Combine Technique(9)



1. There are many ways to accomplish quadrature 3-dB hybrid coupler. The quarter-wave length branch-line coupler composed of four quarter-wave length transmission lines with characteristic impedance of Z0 and Z0/√2 are illustrated in this figure. Input signal at port1 is equally divided into port 2 and port 3 with quadrature-phase.
2. However, the disadvantages of large size and narrow bandwidth limit its practical implement for MMIC integration.

Example 1:
Pre-Distortion Technique

Example 1 : Pre-Distortion Technique(1/4)



$$R_{ds} = \frac{1}{\frac{\partial I_{ds}}{\partial V_{ds}}} = \frac{1}{k \times (V_{CTRL} - V_S - V_{TH})}$$

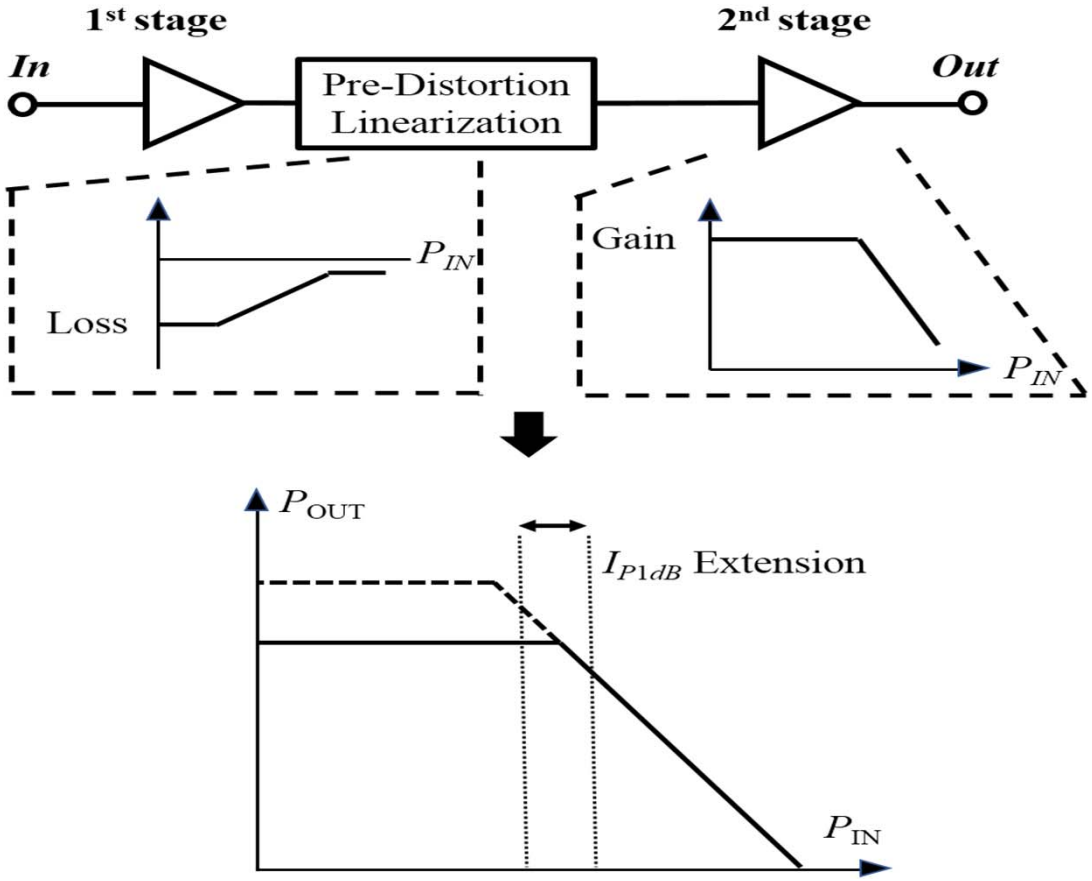
$$|S_{21}| = \frac{2}{\sqrt{\left(2 + \frac{Z_0}{R_{ds}} + \frac{Z_0 R_{off} \omega^2 C_{off}^2}{1 + R_{off}\omega^2 C_{off}^2}\right)^2 + \left(\frac{\omega Z_0 C_{off}}{1 + R_{off}\omega^2 C_{off}^2}\right)^2}}$$

$$IL = 10\log \frac{|R_{ds} // (\frac{1}{j\omega C_{off}} + R_{off})|}{|Z_{gin}| + |R_{ds} // (\frac{1}{j\omega C_{off}} + R_{off})|}$$

(a) Conventional architecture
(b) The equivalent circuit

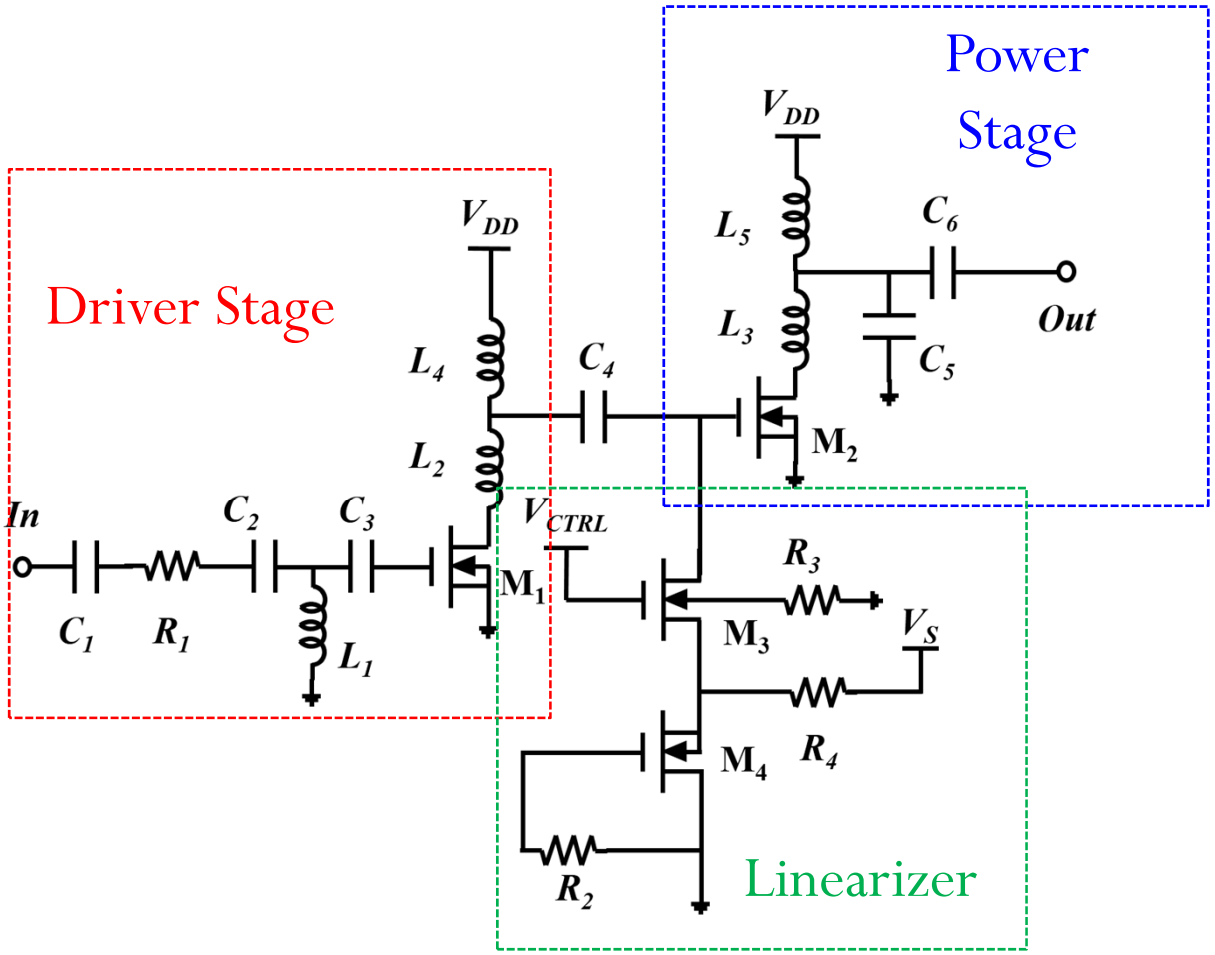
R_{ds} ↑ IL ↓

Example 1 : Pre-Distortion Technique(2/4)



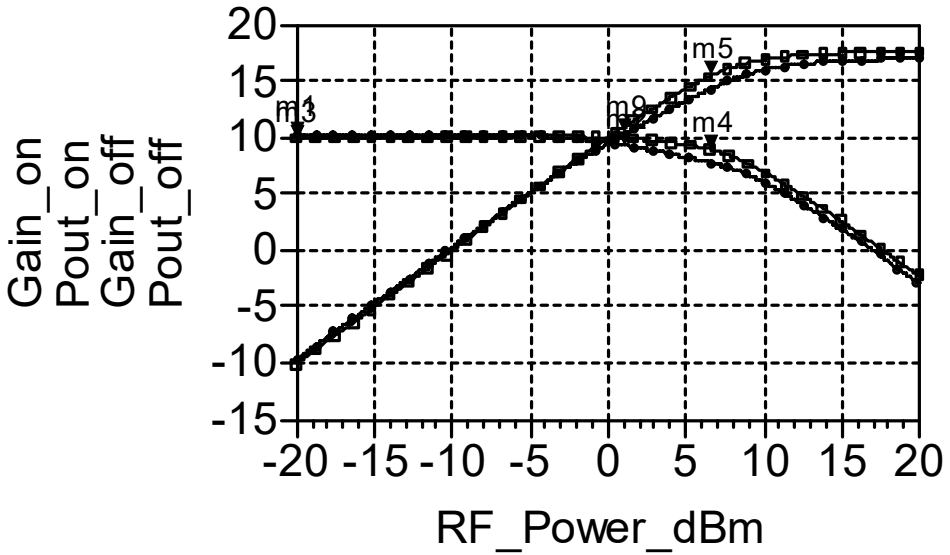
The pre-distortion in two stages PA.

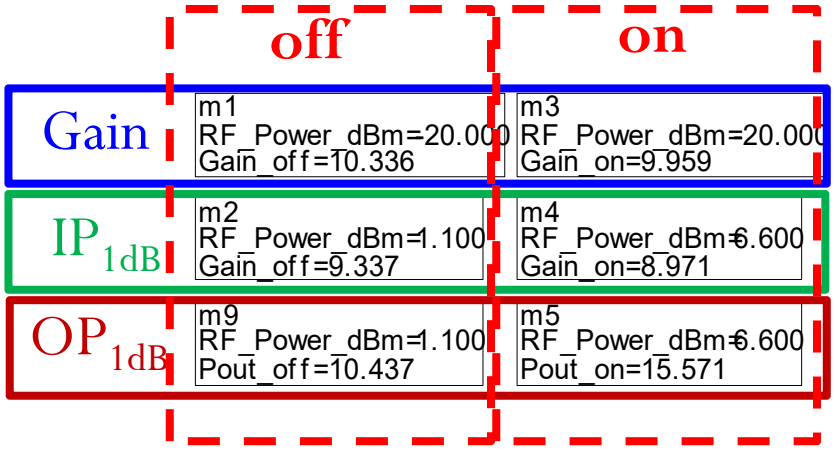
Example 1 : Pre-Distortion Technique(3/4)



The full diagram of the linear PA.

Example 1 : Pre-Distortion Technique(4/4)





The simulated large-signal results.

Summary

- **Several linearity improved techniques of power amplifiers were introduced including feed-forward, feedback, post-/pre-distortion, and derivative superposition techniques.**

- **Various power combine methods such using different amplifier topologies and passive components were detailed.**

Reference

- https://simeneer.blogspot.tw/p/blog-page_4.html. (李健榮 教授-RF Transceiver Module Design/ Multiband RF Transceiver System課程教材)
- RF Microelectronics, Prentice-Hall. Behzad Razavi.
  (代理商: 新月書局)
- Microwave Transistor Amplifiers: Analysis and Design.
  (代理商:高立圖書)
- RF Power Amplifier Design. (張盛富 教授)

寬頻收發關鍵技術模組—
功率放大器預失真線性化技術

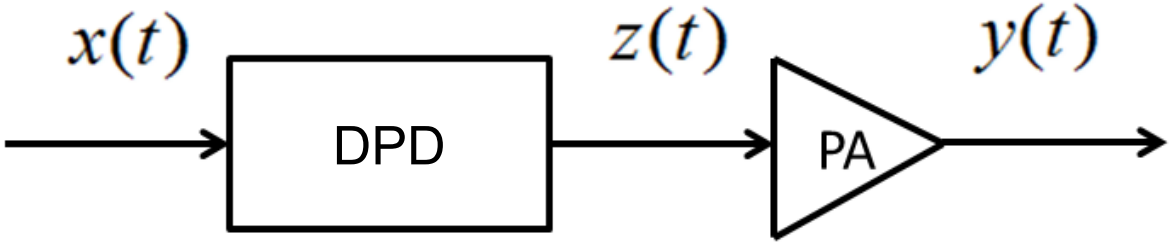
黃建彰
元智大學電機系乙組

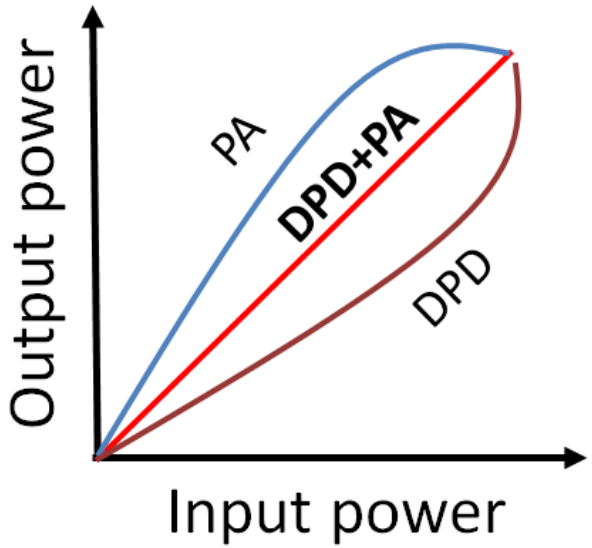
大綱

- 數位預失真線性化技術
  - 查表法
  - 記憶多項式法
- 功率放大器非線性模型
  - 非記憶性非線性模型
  - 記憶性非線性模型
- 記憶多項式描述方式
- 數位預失真線性化軟硬體系統運作

數位預失真線性化技術

將DPD與PA兩個非線性系統組合為一個線性系統，使得功率放大器能操作在靠近飽和區域，同時達到高效率與高線性度特性





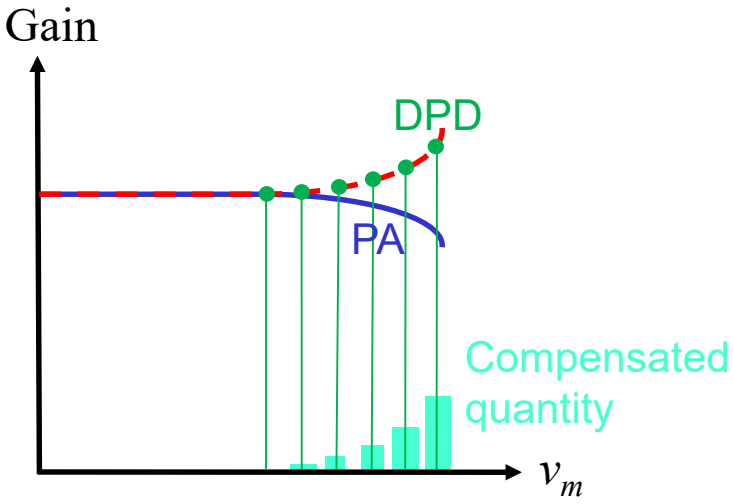
DPD: Digital Pre-Distortion

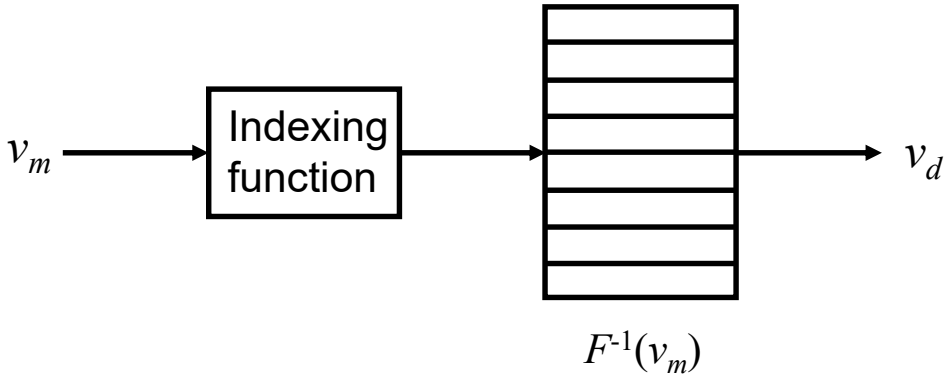
PA: Power Amplifier

如何精準、有效地描述功率放大器的非線性特性，為重要關鍵

數位預失真線性化技術－查表法

查表法 (Look-Up Table, LUT)：量測功率放大器特性函數 $F(v_m)$，計算其反函數$F^{-1}(v_m)$並作量化，儲存於查找表的記憶體內，依據輸入訊號 v_m 的量值找出相對應補償量的記憶體位址，得到預失真後之基頻訊號 v_d。





數位預失真線性化技術－記憶多項式法

記憶多項式法 (Memory Polynomial)：求出放大器多項式的反函數，以反函數補償功率放大器。

- 功率放大器模型分為有記憶性 (memory) 及非記憶性 (memoryless)
- 非記憶性：多項式模型 (polynomial model)、Saleh 模型、Rapp 模型等等。
- 有記憶性：Volterra級數、Wiener和 Hammerstein 模型、和記憶多項式模型等。

非記憶性功率放大器非線性模型

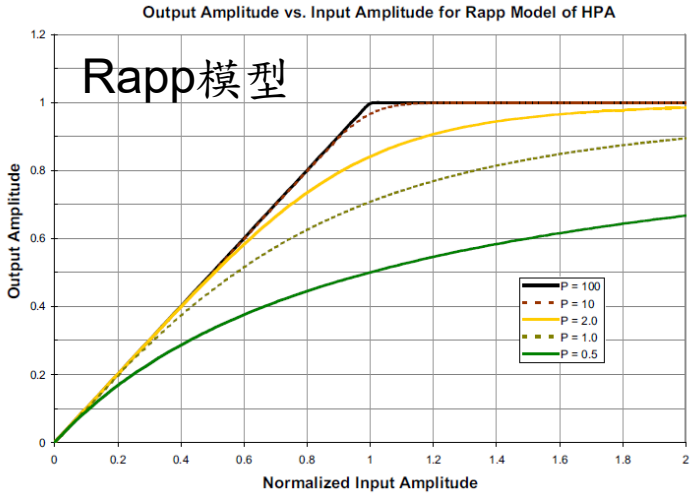
泰勒級數： $v_o = a_o + a_1 v_i + a_2 v_i^{\,2} + a_3 v_i^{\,3} + \ldots\ldots + a_k v_i^{\,k}$

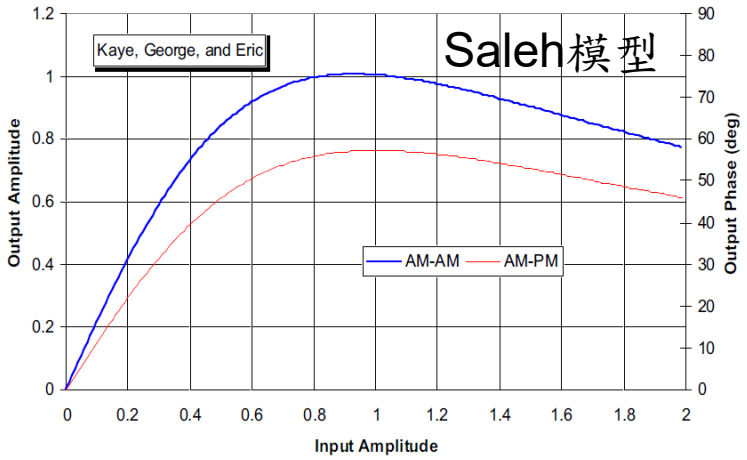
多項式模型： $y(n) = \sum_{K=1}^{K} b_k x(\mathrm{n}) \left| x(n) \right|^{k-1}$

Rapp模型： $V_{out} = \dfrac{V_{in}}{\left[1 + \left(\dfrac{\left| V_{in} \right|}{V_{sat}} \right)^{2p} \right]^{1/2p}}$ ，$\theta = 0$

Saleh模型： $y(n) = \dfrac{\alpha_a x(n)}{\left[1 + \beta_a x(n)^2 \right]}$

$\phi(n) = \dfrac{\alpha_p x(\mathrm{n})}{\left[1 + \beta_p x(n)^2 \right]}$





David Falconer , “System Impairment Model” , Carleton University , 2017.

記憶性功率放大器非線性模型

三階Volterra級數：

$$z(n)=\sum_{q=0}^{Q}h_1(q)x(n-q)+\sum_{q_1,q_2,q_3}^{Q}h_3(q_1,q_2,q_3)\times x(n-q_1)x(n-q_2)x^*(n-q_3)$$

其中 $\{h_1(q)\}_{q=0}^{Q}$ 及 $\{h_3\{q_1,q_2,q_3)\}_{q_1,q_2,q_3=0}^{Q}$ 決定非線性系統的特性

$\{h_3\{q_1,q_2,q_3)\}_{q_1,q_2,q_3=0}^{Q}$ 表示 q_1, q_2, q_3從 0 到 Q 形成的排列組合

假如 $Q=0$，級數會變成非記憶性多項式。若令 $q_1=q_2=q_3$ 且非零，其他項為零，則可改寫成

$$z(n)=\sum_{q=0}^{Q}[\mathrm{h}_1(q)x(n-q)+h_3(q,q,q)x(n-q)\left|x(n-q)\right|^2]$$

記憶多項式描述方式

$$y_{MP}(\mathrm{n}) = \sum_{k=0}^{K-1}\sum_{m=0}^{M-1} a_{km}\, x(n-m)\left|x(n-m)\right|^{k}$$

$$x_{MP}(\mathrm{n}) = \sum_{k=0}^{K-1}\sum_{m=0}^{M-1} d_{km}\, y_{ss}(n-m)\left|y_{ss}(n-m)\right|^{k}$$

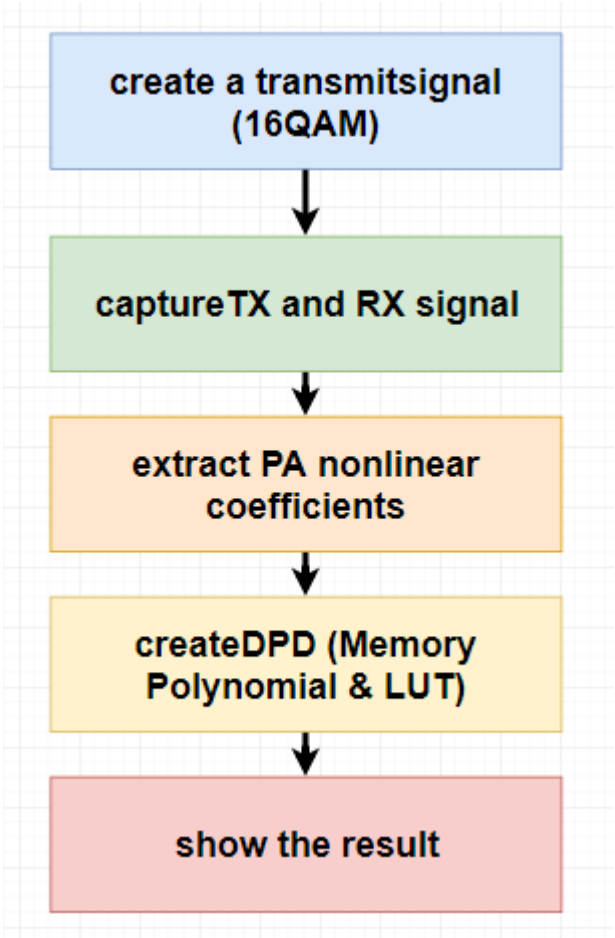
$$y_s(n) = y(n)/G \qquad y_{ss}(n) = y_s(n+offset)$$

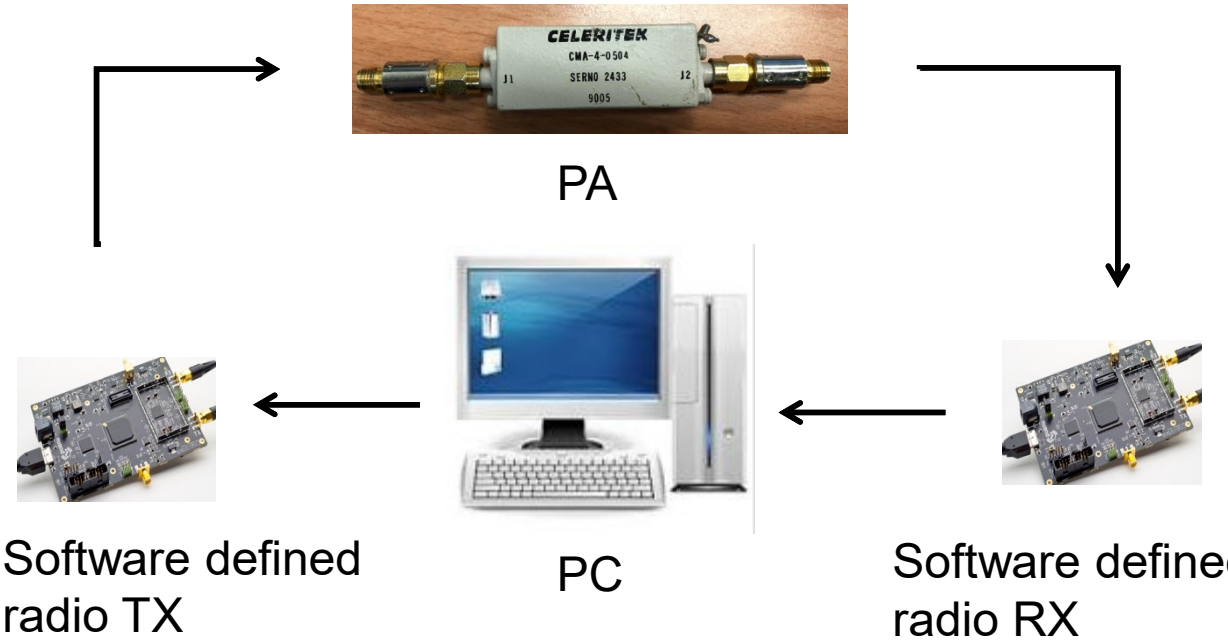
MATLAB 實現方式：$$x_{MP}(\mathrm{n}) = \sum_{k=1}^{K}\sum_{m=1}^{M} d_{km}\, y_{ss}(n-m+1)\left|y_{ss}(n-m+1)\right|^{k-1}$$

M. Morgan, Z. Kim, and Pastalan. “A Generalized Memory Polynomial Model for Digital Predistortion of RF Power Amplifiers,” *IEEE Trans. on Signal Processing*, vol. 54, no. 10, Oct. 2006.

K. Schutz and D. Benson, “Adaptive DPD Design,” Mathworks, 2014.

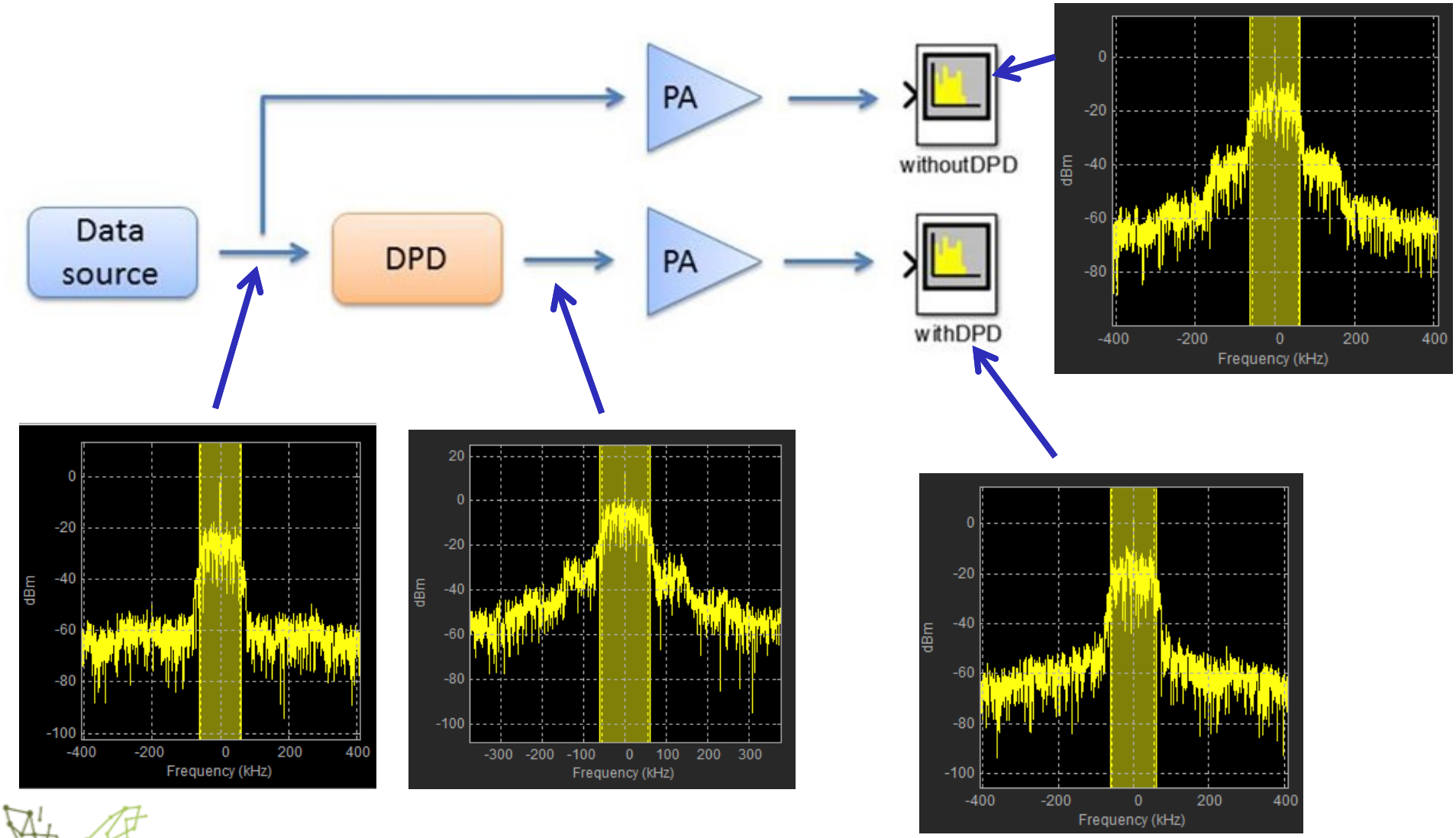
數位預失真線性化軟硬體系統運作流程





Step 1 : create a transmit signal (16QAM)
Step 2 : capture TX and RX signal
Step 3 : extract PA nonlinear coefficients
Step 4 : create DPD (Memory Polynomial & LUT)
Step 5 : show the result

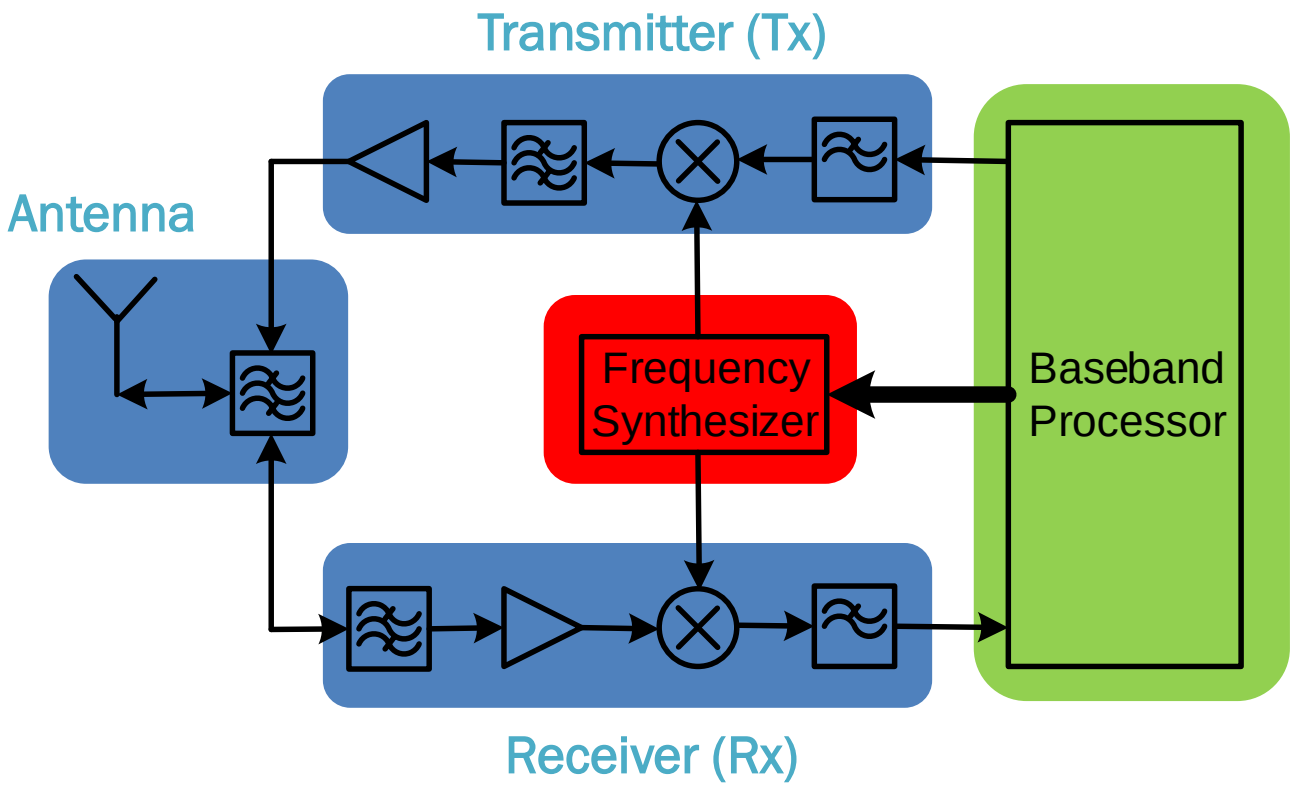
數位預失真線性化結果呈現



mm-wave Frequency Synthesizers

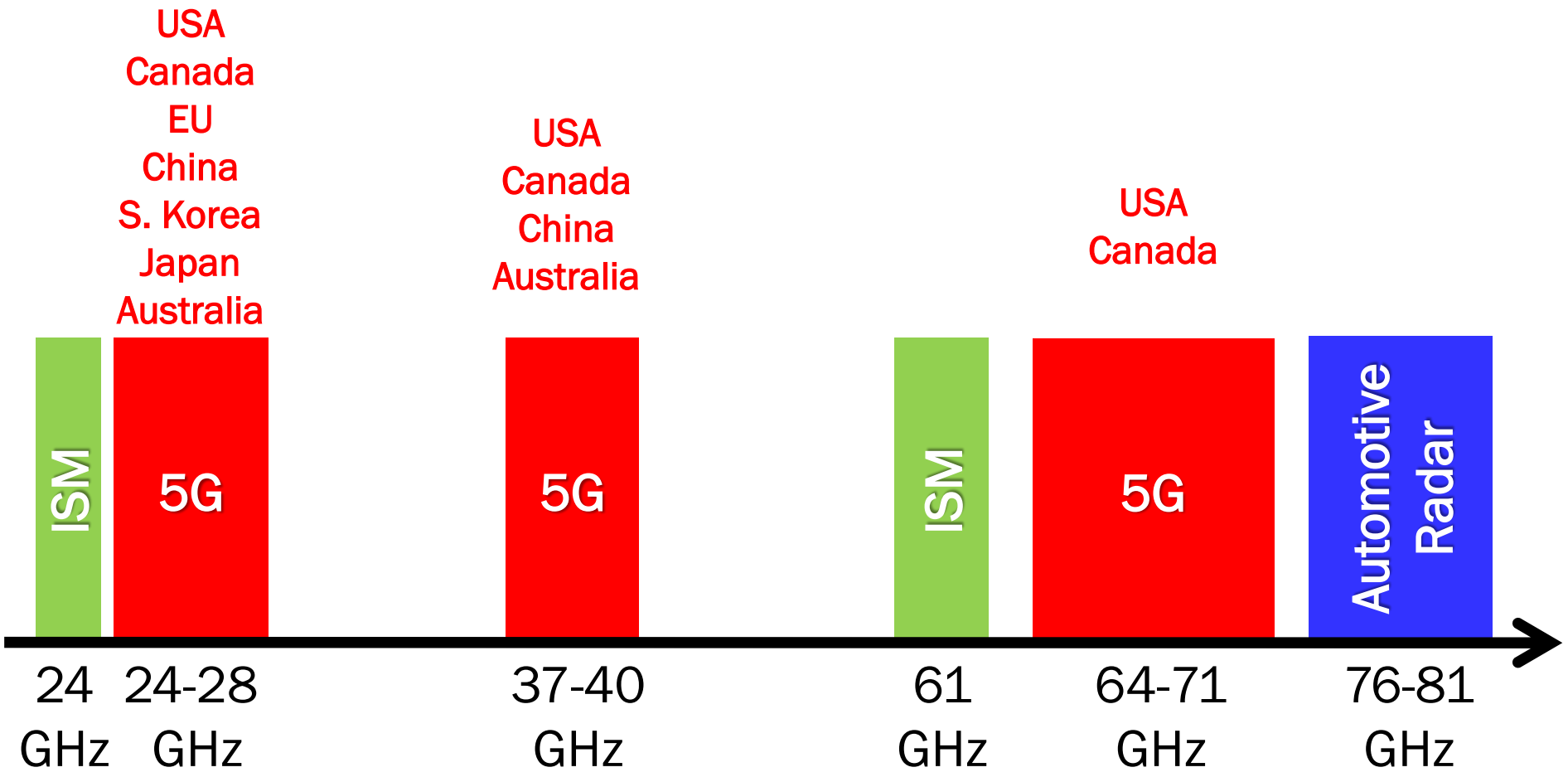
彭康峻
國立高雄科技大學
電腦與通訊工程系

Wireless Communication System

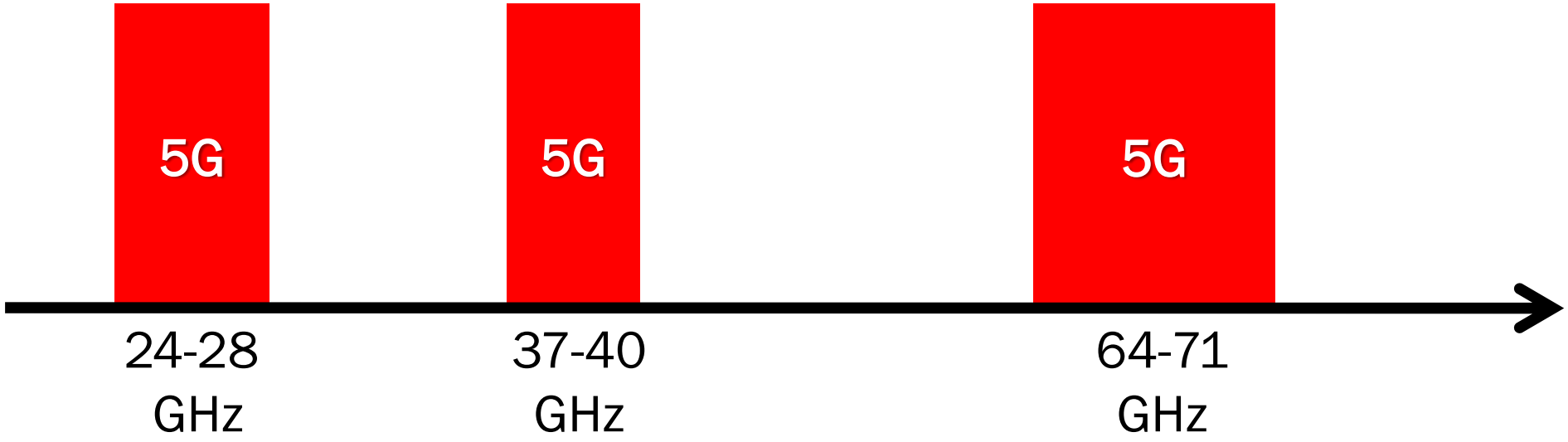


More advanced wireless systems require higher performance frequency synthesizers.

mm-Wave Bands



Operating Range Issue for 5G



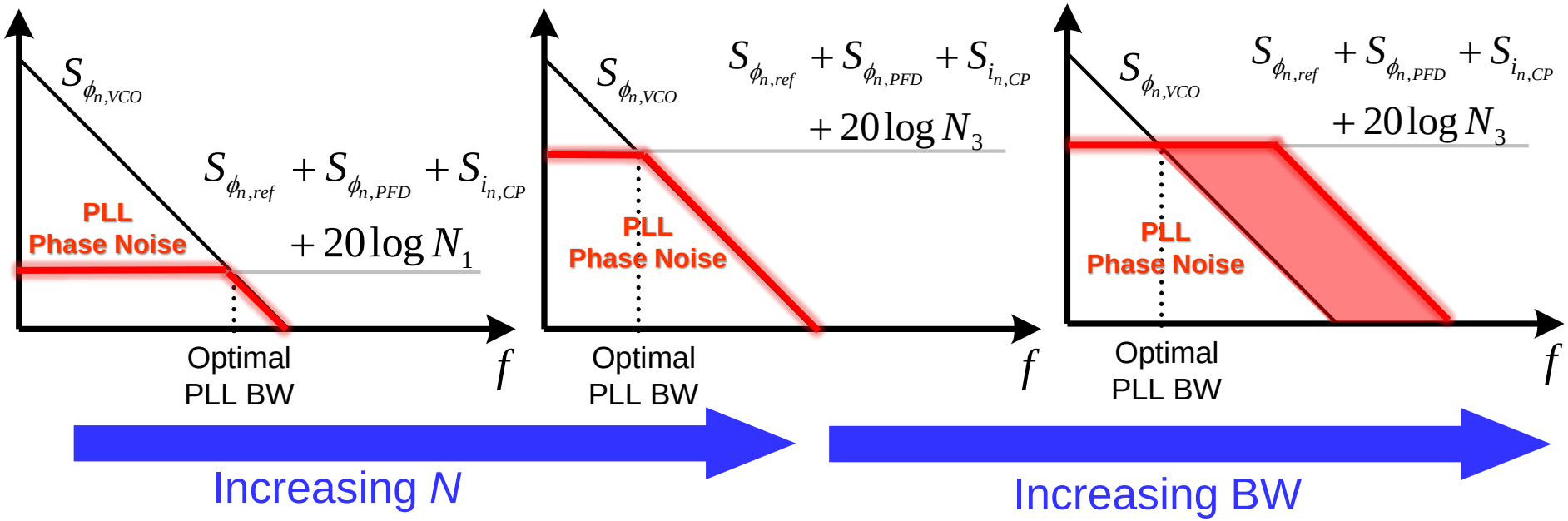
For 5G applications, conventional frequency synthesizers with a single VCO is incapable of operating from 24-71 GHz with a fractional bandwidth up to 99 %.

Operating Range Issue for Starlink

Uplink	Downlink
14.0-14.5 GHz	10.7-12.7 GHz
27.5-29.1 GHz	17.8-18.6 GHz
29.5-30.0 GHz	18.8-19.3 GHz
47.2-52.4 GHz	37.5-42.5 GHz

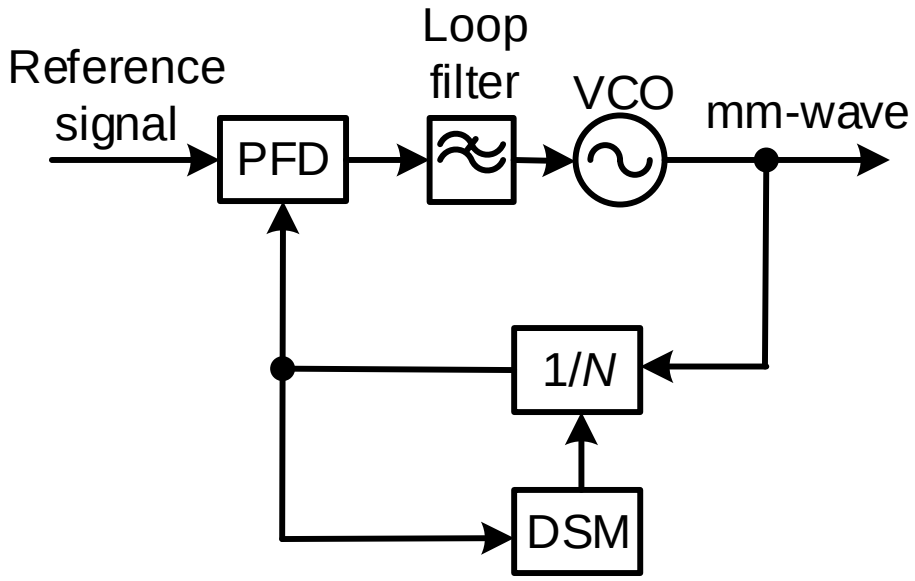
For Starlink system (potential for 6G applications), the fractional bandwidth of frequency synthesizer is up to 132 % (10.7-52.4 GHz).

Phase Noise Degradation in mm-Wave Bands



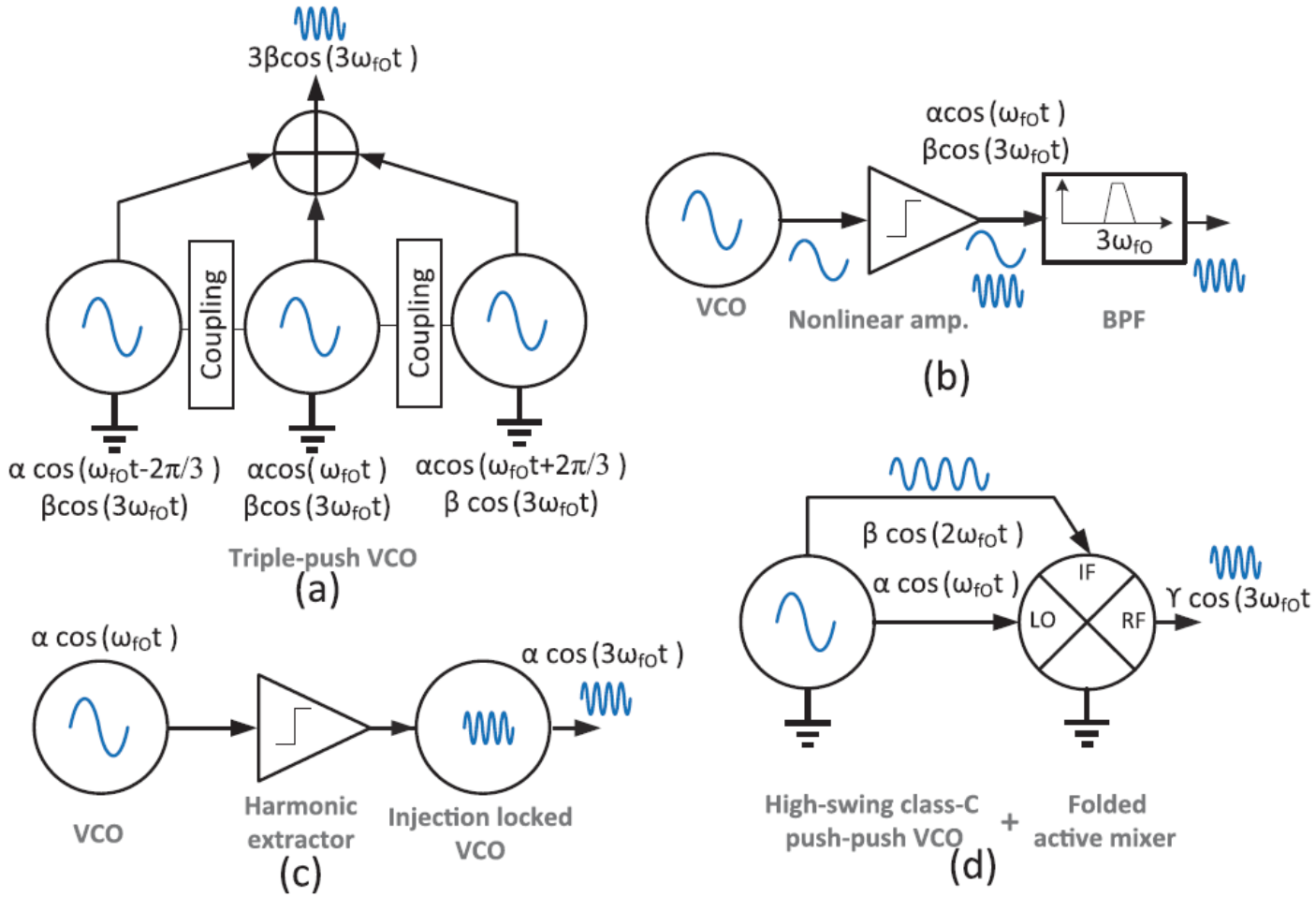
- mm-wave frequency synthesizers suffer poor phase noise due to the large division *N*.
- The 20log*N* gain greatly increases the DSM quantization noise and the phase noise from reference signal and PLL components.

Single-stage mm-Wave Frequency Synthesizer



- Fractional-*N* frequency synthesizer is the key to synthesize mm-wave signal with acceptable resolution.
- The phase noise gain of frequency divider, PFD and the reference signal of an mm-wave frequency synthesizer is up to about 20log(71GHz/40MHz)=65 dB.
- The poor phase noise performance of the mm-wave VCO and the high divide-by-N make it difficult to optimize the loop bandwidth.

mm-Wave VCO Topologies



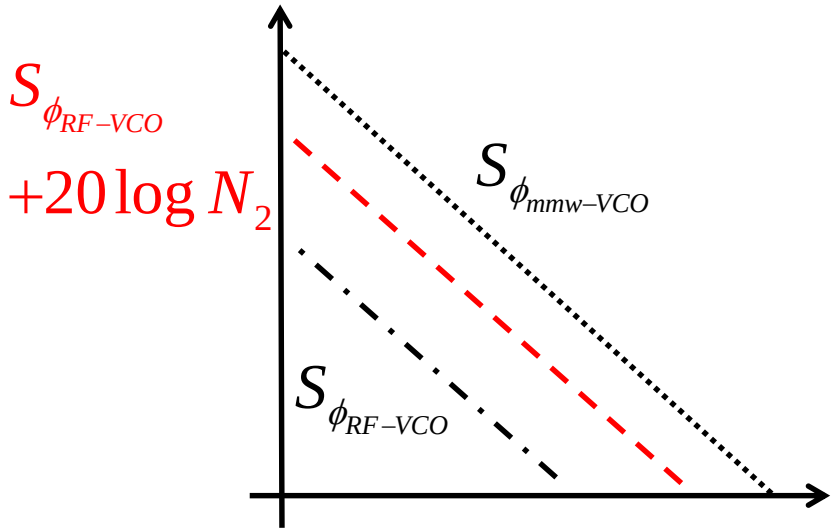
A. H. Masnadi Shirazi et al., "On the Design of mm-Wave Self-Mixing-VCO Architecture for High Tuning-Range and Low Phase Noise," in IEEE Journal of Solid-State Circuits, vol. 51, no. 5, pp. 1210-1222, May 2016.

Phase Noise of mm-Wave VCO

$$S_{\phi_{n,VCO}}(f) = \frac{FkTB}{2P_{avs}}\left[\frac{1}{f^3}\frac{f_o^{\,2} f_c}{4Q^2} + \frac{1}{f^2}\left(\frac{f_o}{2Q}\right)^2 + \frac{f_c}{f} + 1\right]$$

f_c : flicker corner frequency

f_o : operating frequency of VCO



$$f_{mmw} = N_2 f_{RF}$$

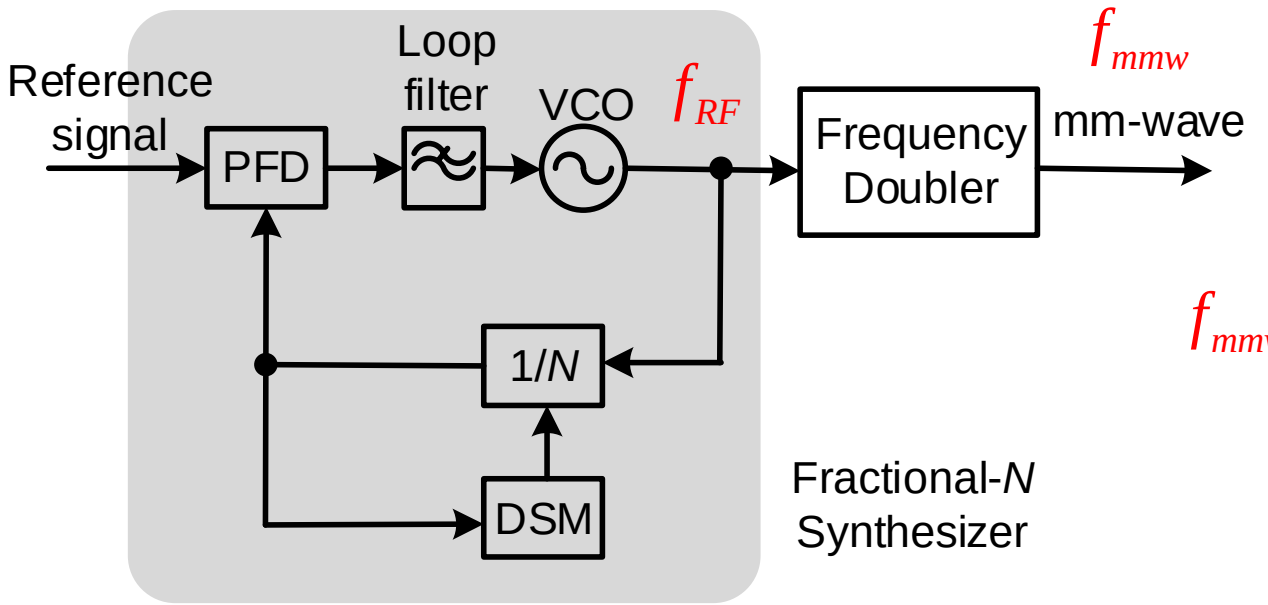
Performance Comparison of 60 GHz VCO Topologies

NKUST 國立高雄科技大學

Parameters	Active-mixer 3H-VCO	Passive-mixer 3H-VCO	Active-mixer 2H-VCO	Passive-mixer 2H-VCO	F-VCO
Mixer gain (V/A Ohm) *	**152.46**	**28.60**	**150**	**28.52**	**NA**
PN (dBc/Hz) @ 1 MHz	–102.4	–101.5	–97.2	–96.8	–94.7
FTR %	10.3	10	8.3	5.8	4.0
Single-ended voltage Swing (mV_{pk-pk})	900	900	900	900	900
Power (core) (mW)	18.5	17.4	21.4	16.2	16.36
Power (buffer) (mW)	10.3	25.8	10.4	11.2	4.28
Total power (mW)	28.8	43.2	31.4	24.4	20.64
FoM (dBc/Hz) (core) @ 60 GHz	–185.3	–184.6	–179.43	–180.26	–178.13
FoM (dBc/Hz) (core+buffer)	–183.36	–180.7	–177.77	–178.08	–177.12
FoM_T (dBc/Hz) (core+buffer)	–183.62	–180.7	–176.15	–173.04	–169.16

A. H. Masnadi Shirazi et al., "On the Design of mm-Wave Self-Mixing-VCO Architecture for High Tuning-Range and Low Phase Noise," in IEEE Journal of Solid-State Circuits, vol. 51, no. 5, pp. 1210-1222, May 2016.

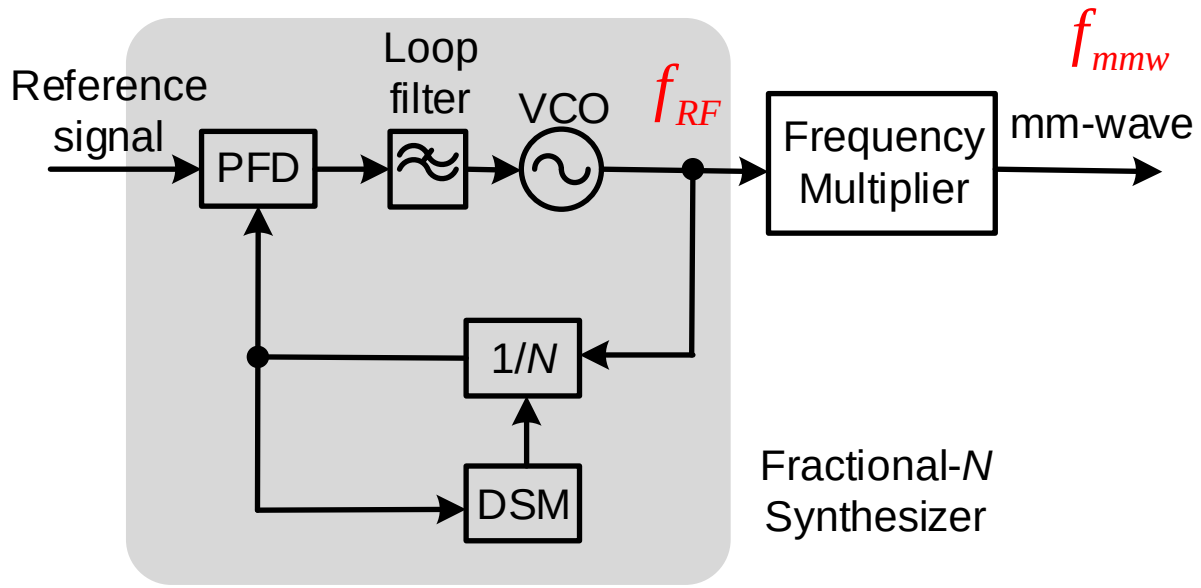
mm-Wave Frequency Synthesizer with Frequency Doubler



$$f_{mmw} = 2 f_{RF}$$

- The doubled output frequency avoid the LO pulling issue.
- The frequency doubler can be realized by using push-push architecture.

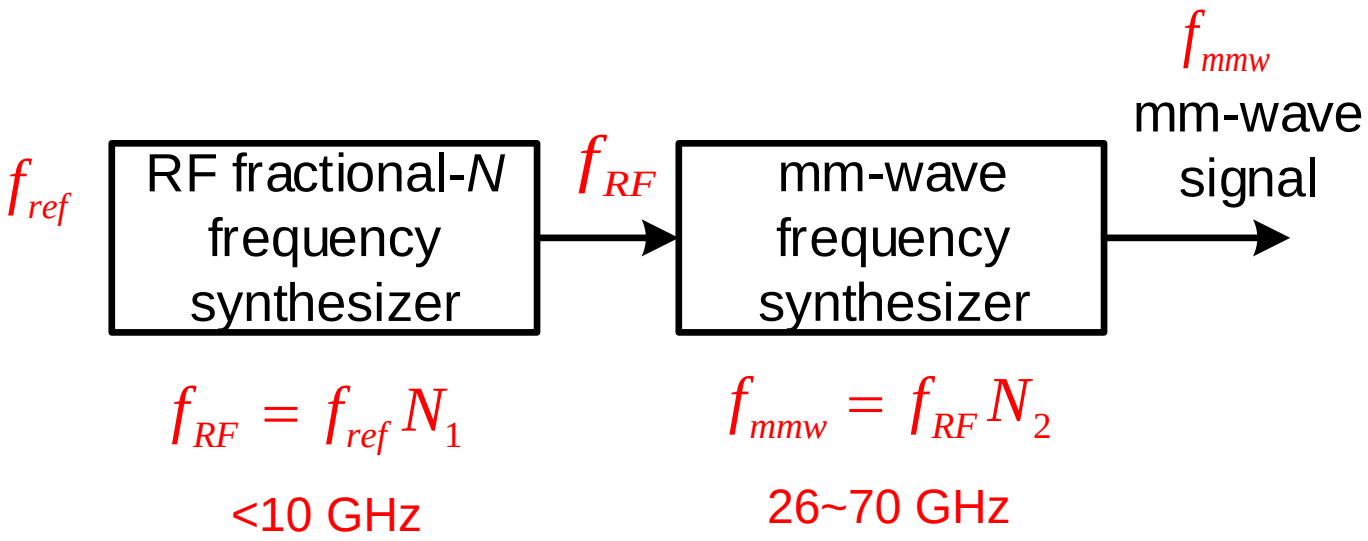
mm-Wave Frequency Synthesizer with Frequency Multiplier



$$f_{mmw} = N_2 f_{RF}$$

- The frequency multiplication avoid the LO pulling issue.
- The frequency multiplier can be realized by using injection-locking techniques or an additional PLL.
- The phase noise performance of the VCO can be improved.

Synthesizer-based Frequency Multiplier



- This architecture can be regarded as a cascaded frequency synthesizer.
- The output signal of the 1st stage fractional-*N* synthesizer serves as the reference signal of the 2nd stage mm-wave synthesizer.
- The loop bandwidth of each stage synthesizer can be optimized according to the phase noise performance of the VCO.

Optimization of Loop Bandwidth & Phase Noise Performance

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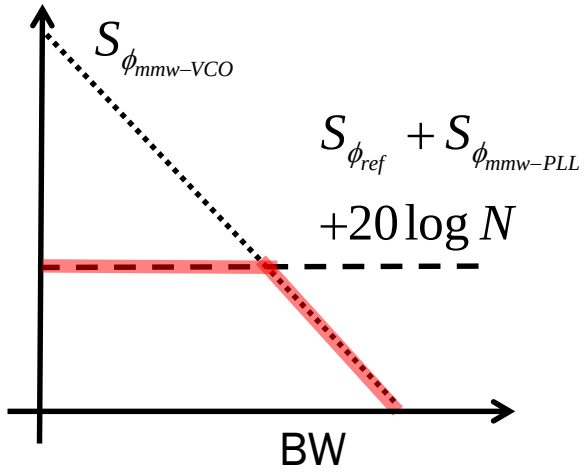
Single stage mm-wave synthesizer

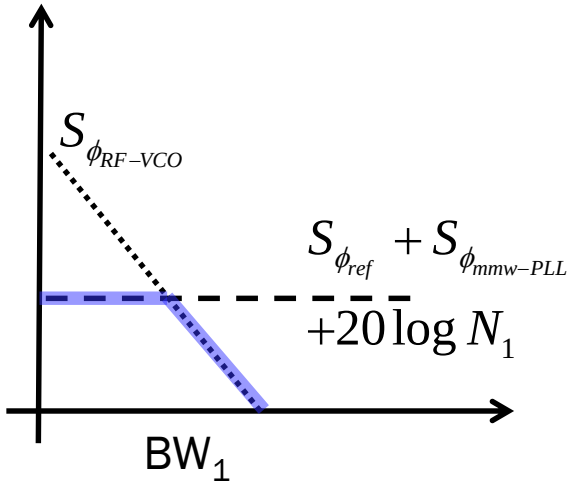


Cascaded mm-wave synthesizer

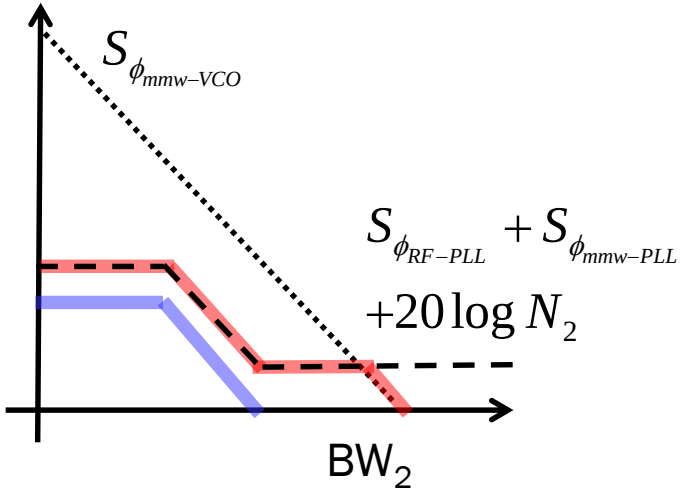
$N = N_1 \times N_2$

$N_1 > N_2$

$BW_2 > BW_1$

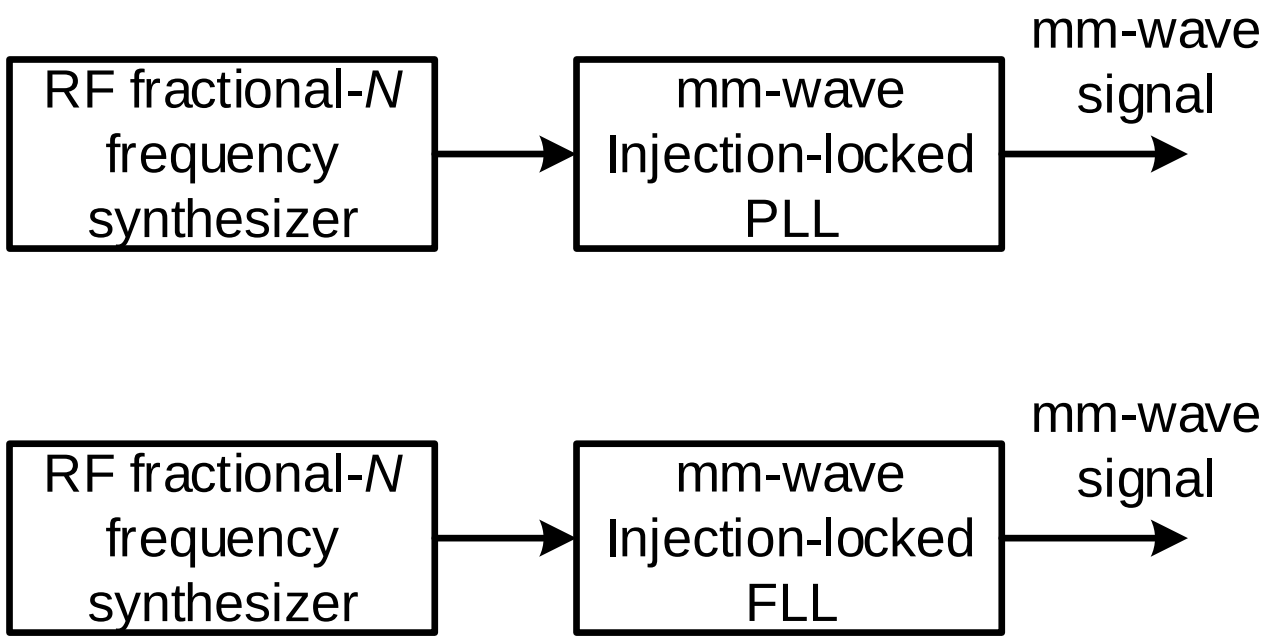


First stage

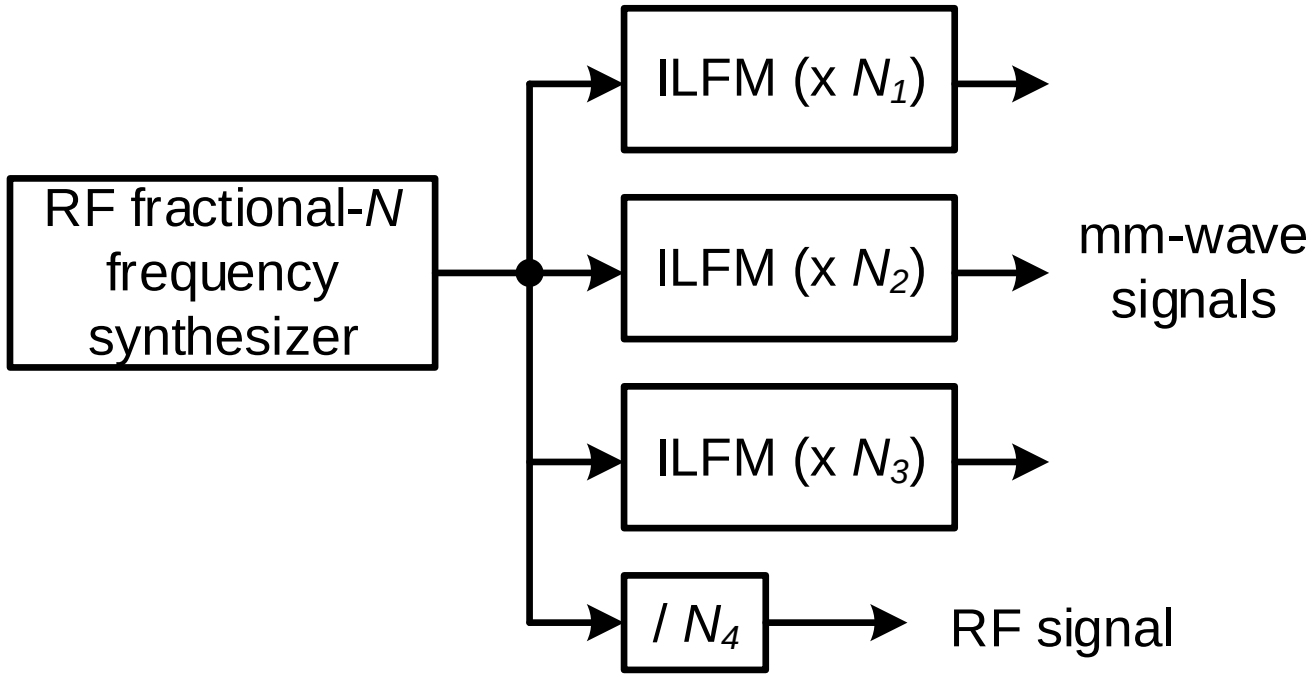


Second stage

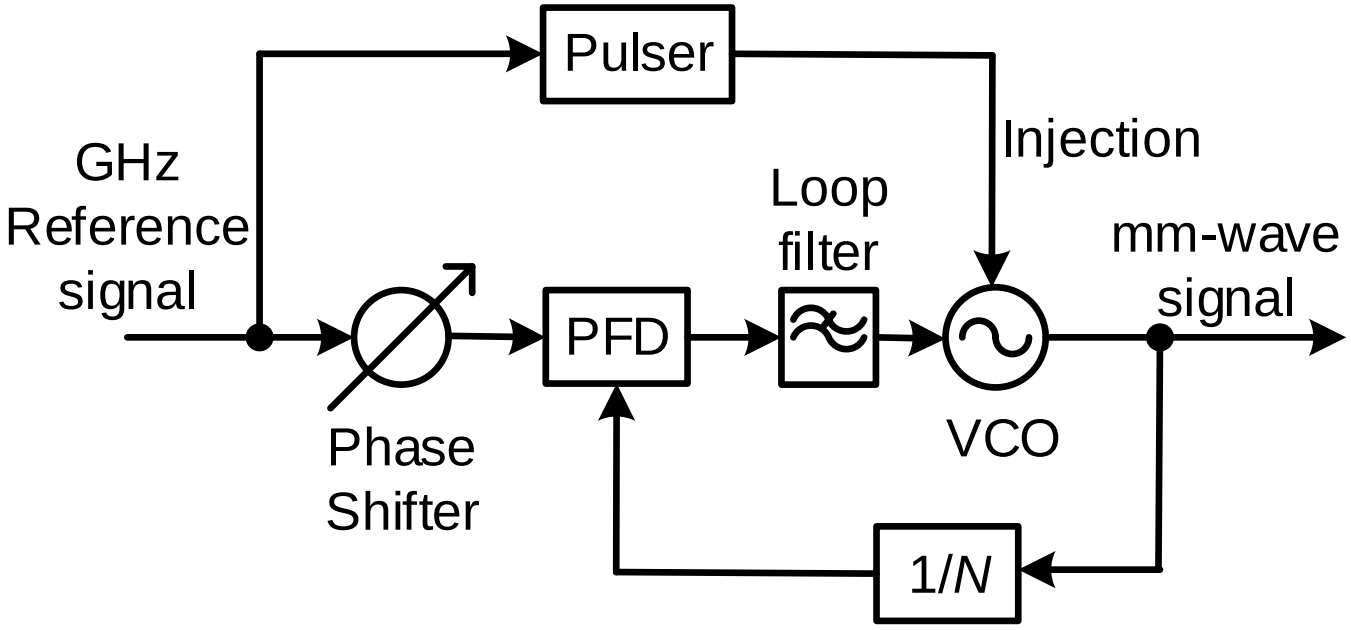
Injection-locked-loop-based Frequency Multiplier (ILFM)



mm-wave Synthesizer with Wide Operating Bandwidth

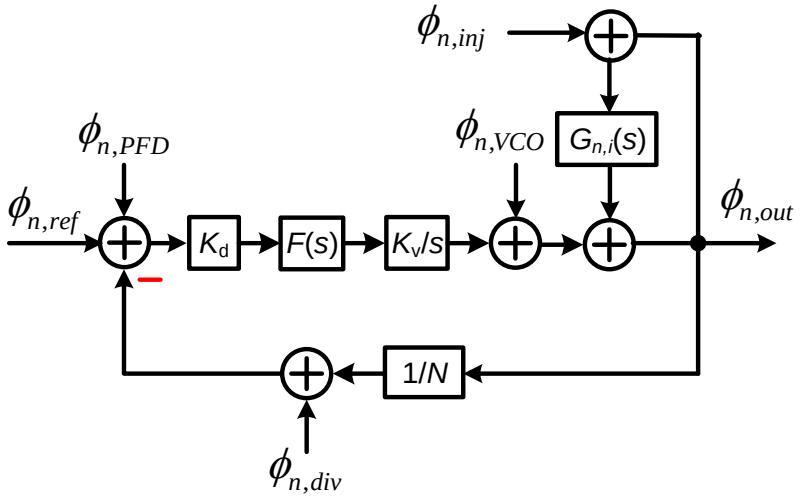


Injection-locked PLL



- The pulse generator generates millimeter wave harmonic signals whose frequency is N times the frequency of the reference signal.
- The phase shifter is used to align the phase of the injected harmonic signal and the one of the VCO output signal.

Model of Injected PLL

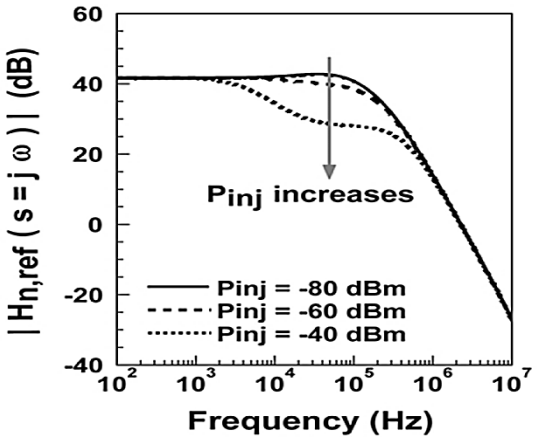


$$G(s)=\frac{K_d K_v F(s)}{s}$$

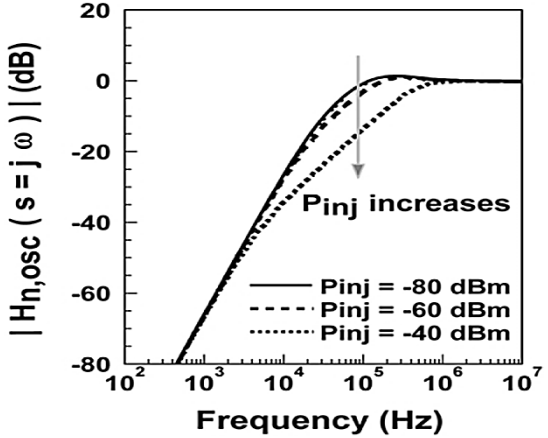
$$G_{n,i}(s)=\frac{\omega_{LR}\cos\alpha_\infty}{s}$$

$$\phi_{n,\text{out}}(s)=H_{n,ref}(s)\left[\phi_{n,ref}(s)+\phi_{n,\text{PFD}}(s)+\phi_{n,\text{div}}(s)\right]+H_{n,inj}(s)N\phi_{n,ref}(s)+H_{n,osc}(s)\phi_{n,o}(s)$$

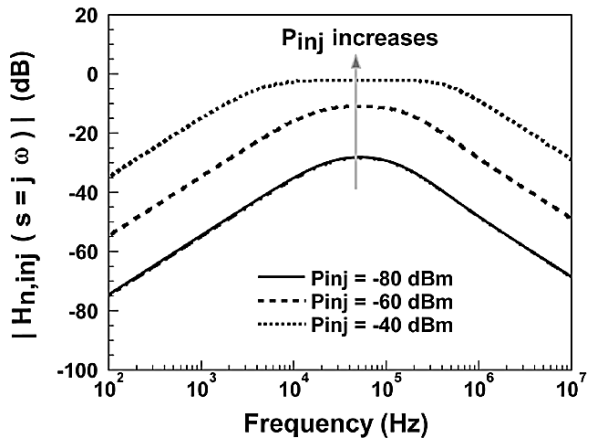
$$H_{n,ref}(s)=\frac{G(s)H_{n,o}(s)}{1+G(s)H_{n,o}(s)/N},$$



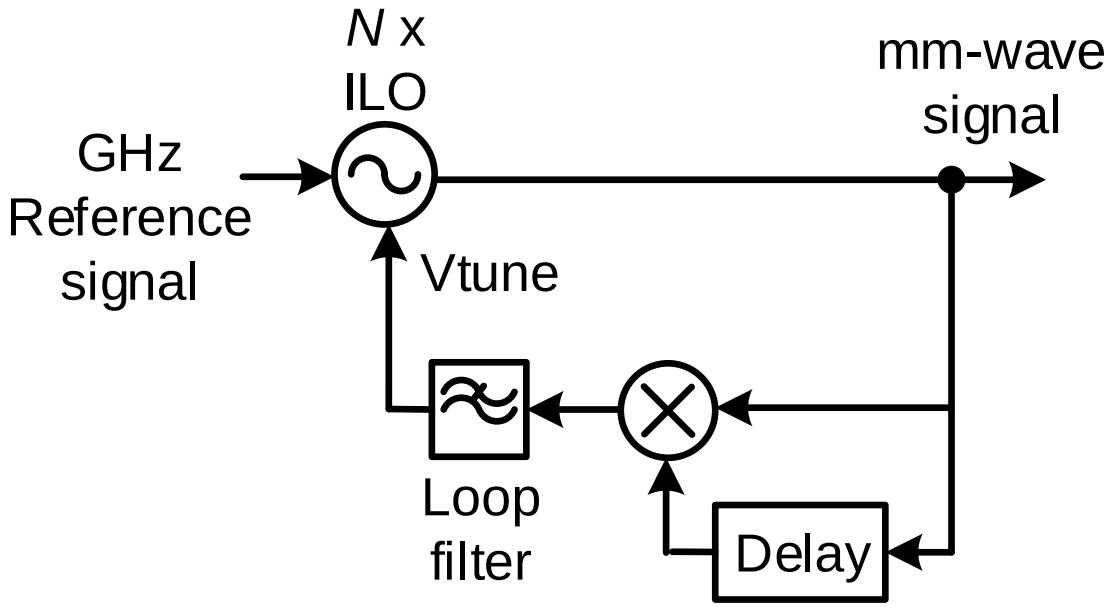
$$H_{n,osc}(s)=\frac{H_{n,o}(s)}{1+G(s)H_{n,o}(s)/N},$$



$$H_{n,inj}(s)=\frac{H_{n,i}(s)}{1+G(s)H_{n,o}(s)/N}$$

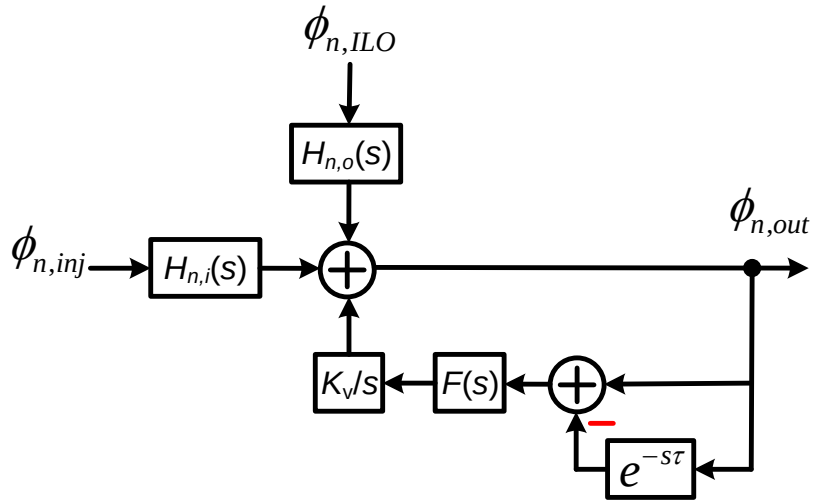


Injection-locked FLL



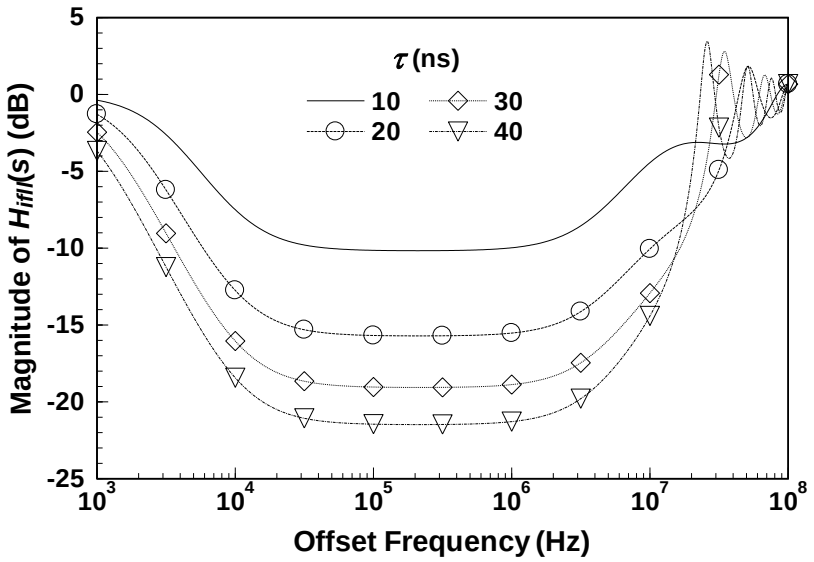
- The delay element is the key of the mm-wave frequency-locked loop (FLL).
- The delay element should be low noise while providing several ns delay for sufficient phase noise reduction.

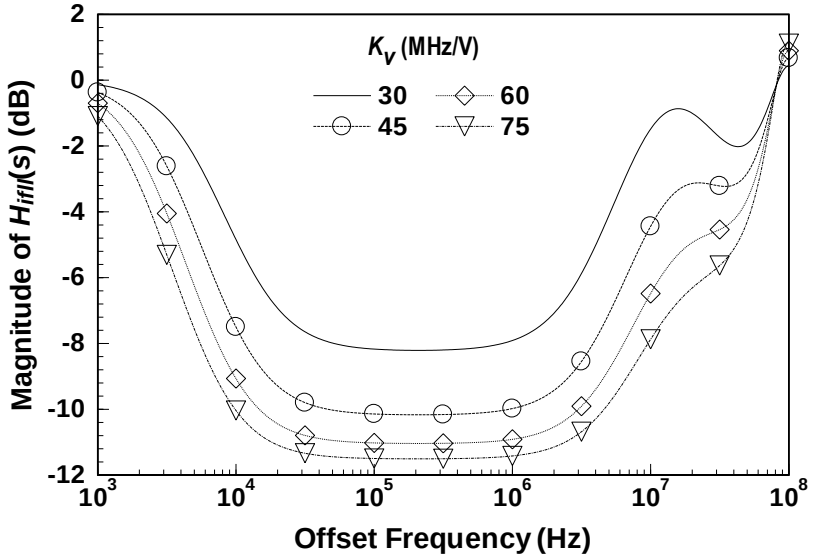
Model of Injected FLL



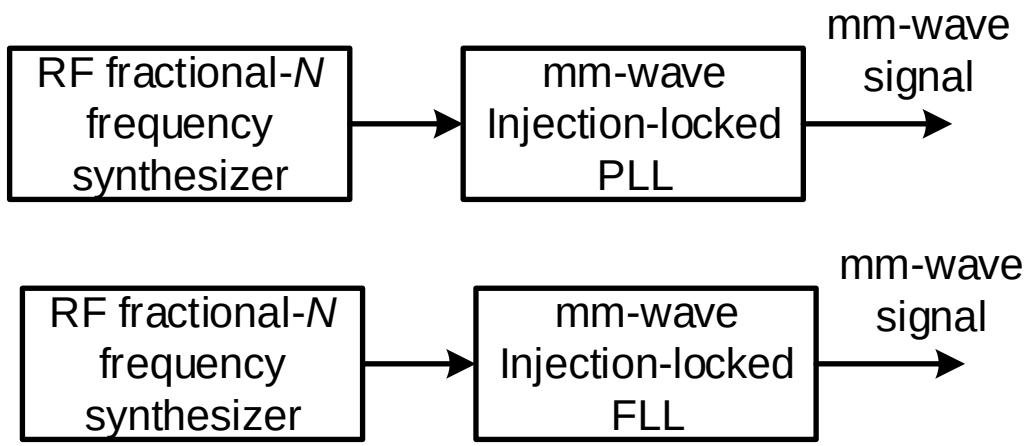
$$\phi_{n,out} = \left[\phi_{n,\mathrm{ILO}} H_{n,\mathrm{o}}(s) + \phi_{n,\mathrm{inj}} H_{n,i}(s)\right] H_{ifll}(s)$$

$$H_{ifll}(s) = \frac{s}{2\pi K_v F(s)\left[1 - e^{-s\tau}\right] - s}$$

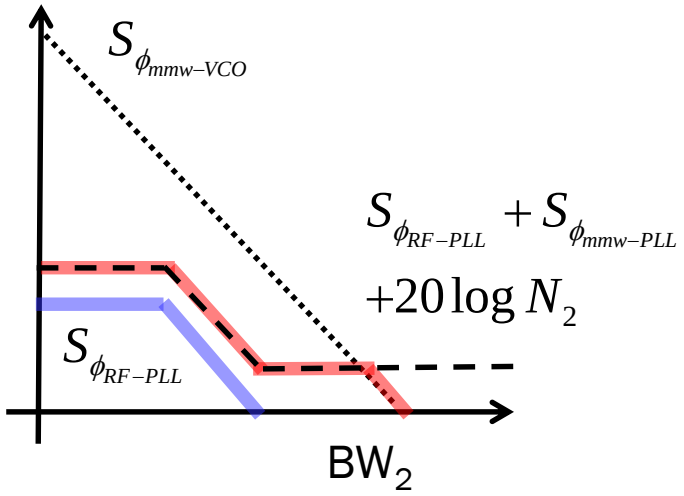




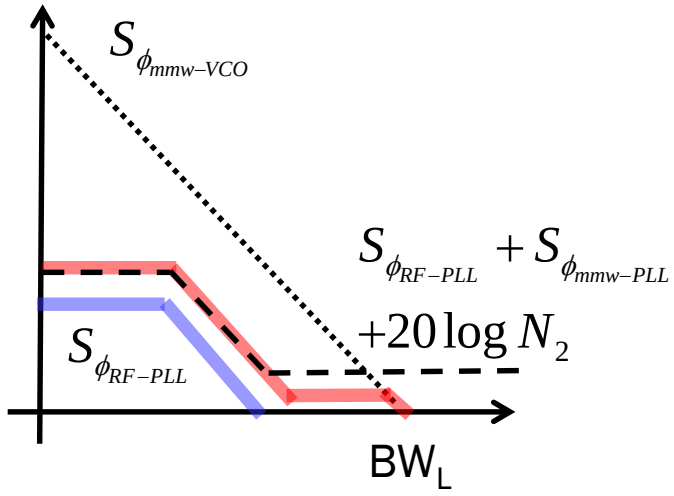
Injection-locked-loop-based Frequency Multiplier



Phase noise of second stage



$BW_L < BW_2$



$BW_L > BW_2$

Conclusion

- The issue of mm-wave frequency synthesizer includes LO pulling effects, operating range and phase noise performance.
- The operating range of synthesizer can be extended by using frequency-offset technique.
- Both the LO pulling effects and the phase noise performance issue of mm-wave frequency synthesizer can be overcame by using cascaded injection-locking synthesizer.